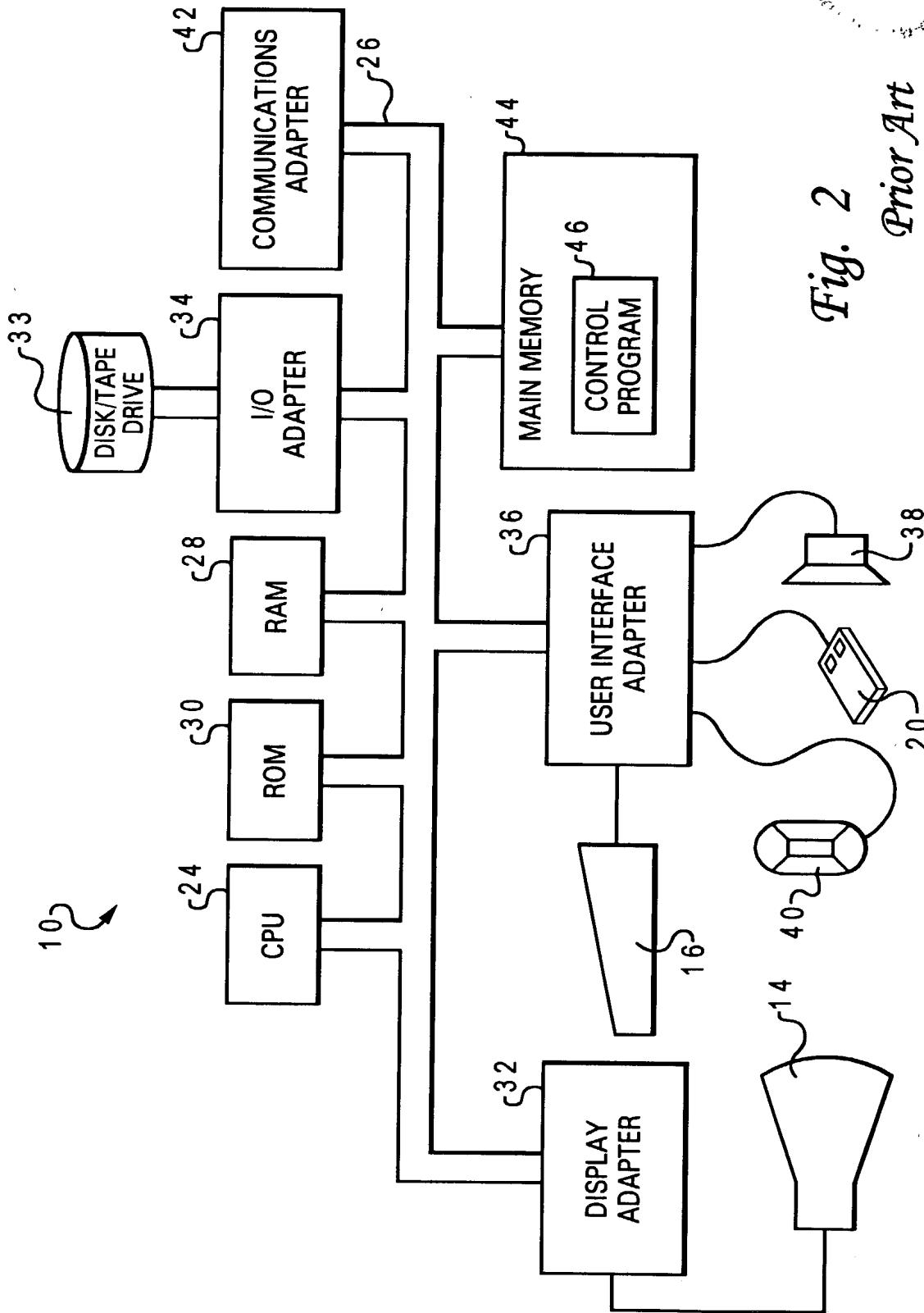


Fig. 1
Prior Art

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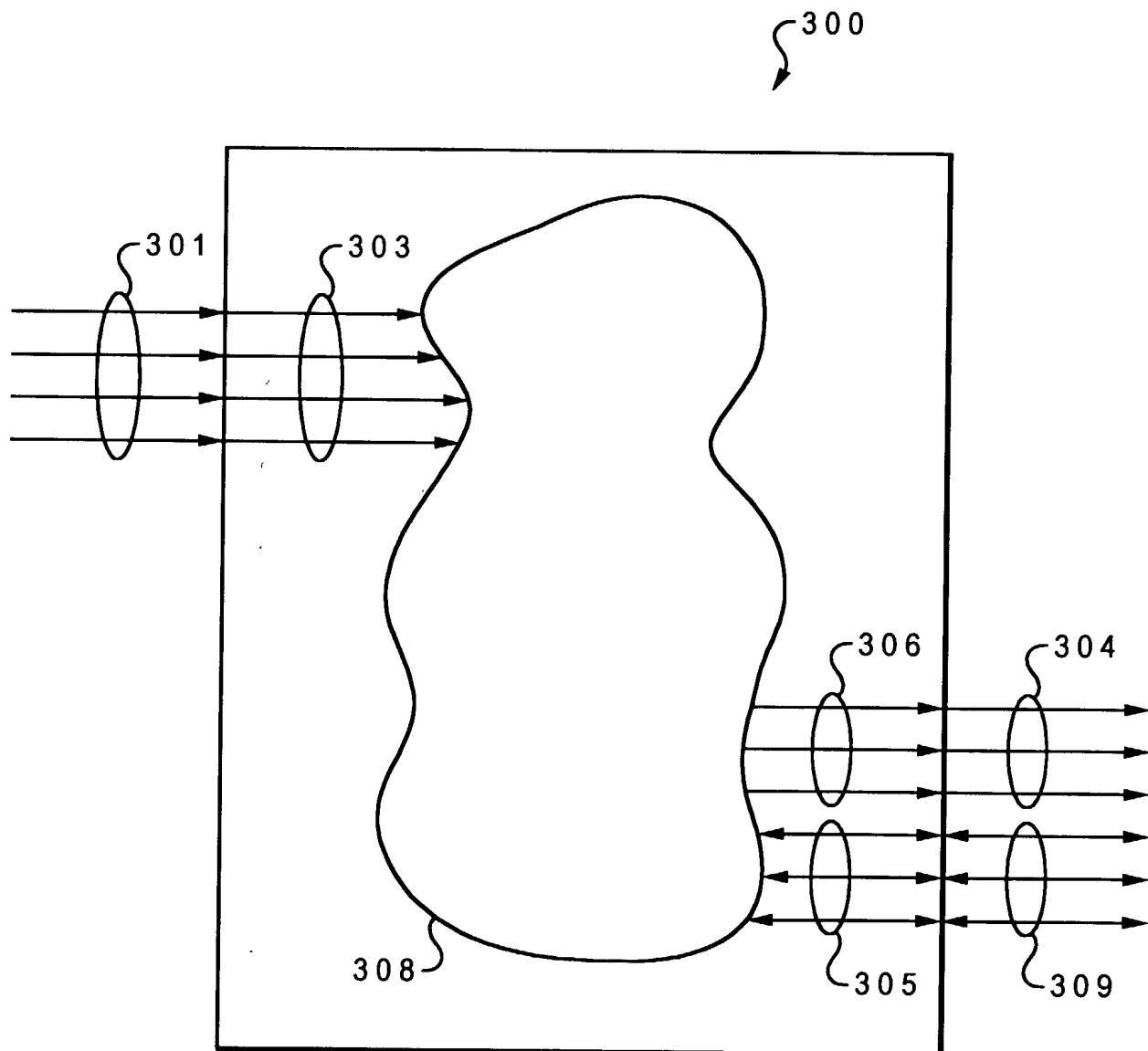


Fig. 3A

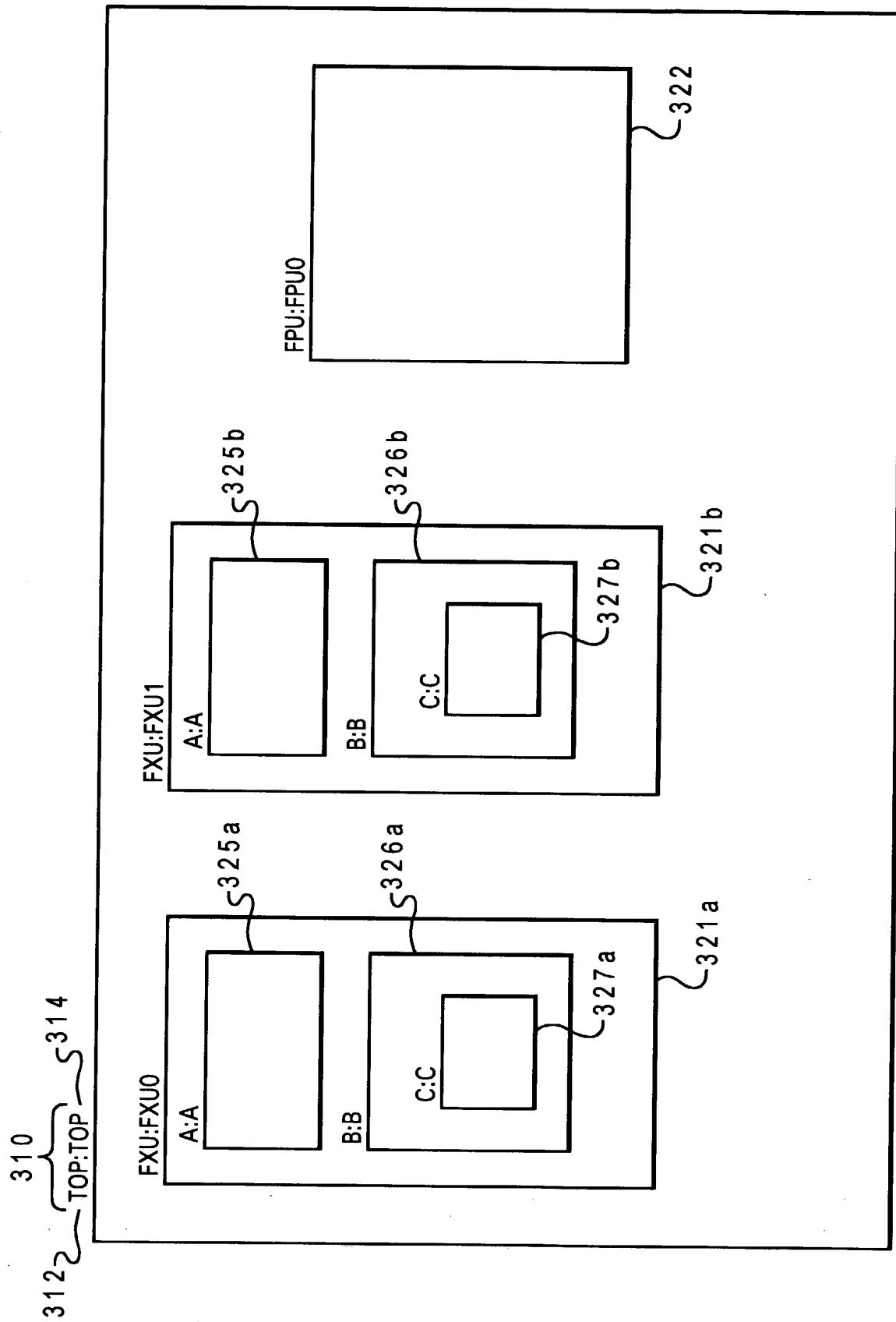


Fig. 3B

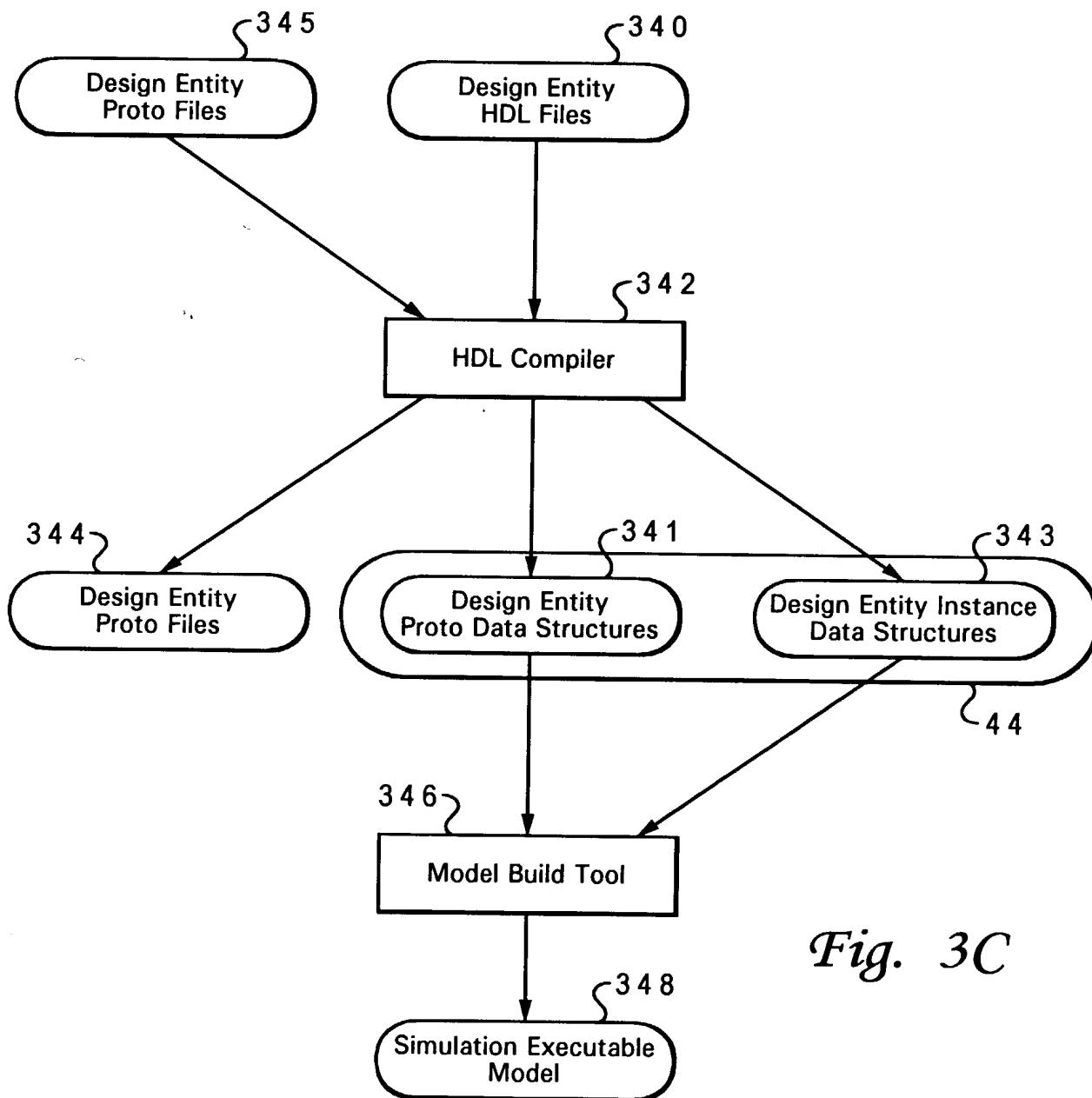
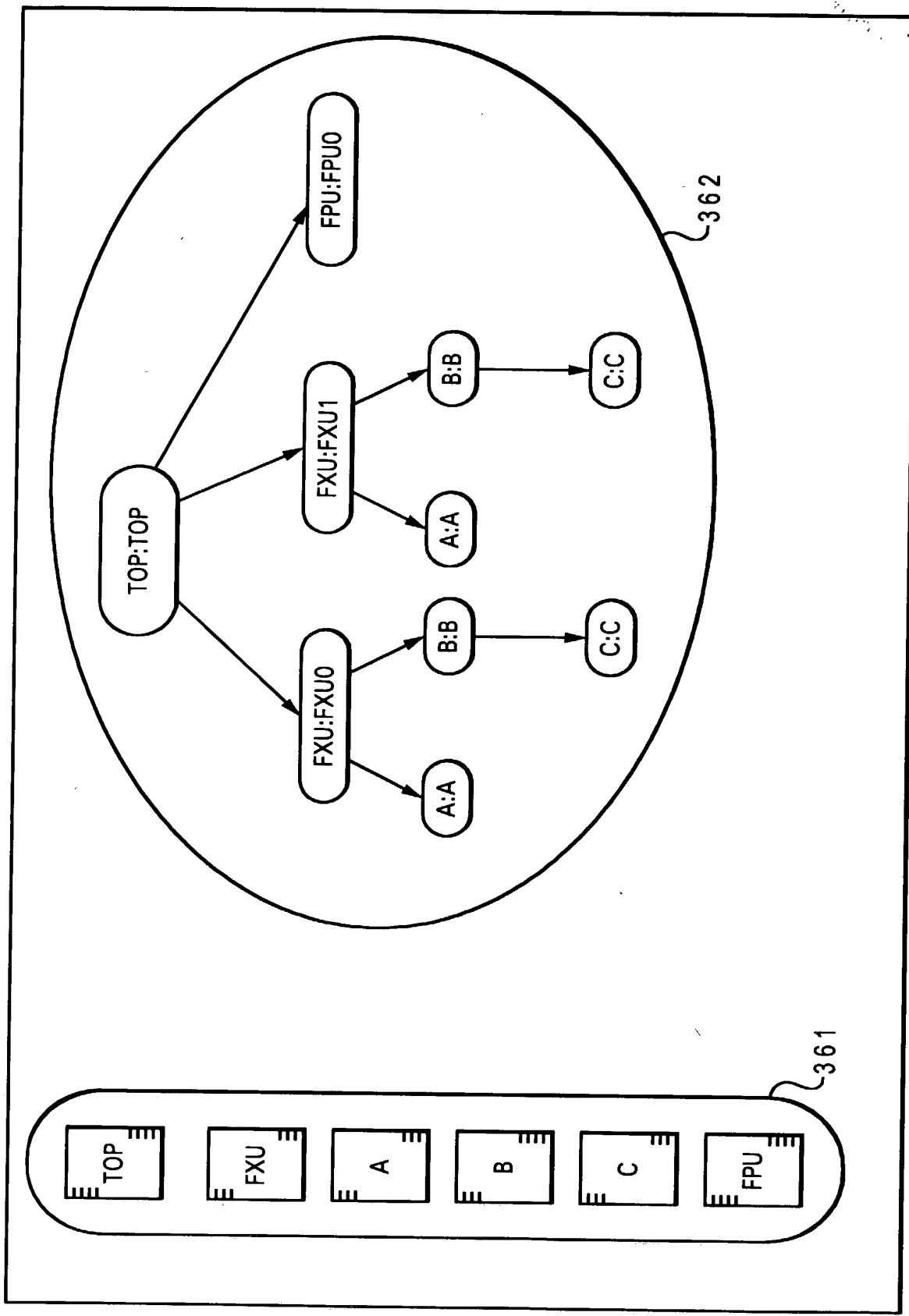


Fig. 3C

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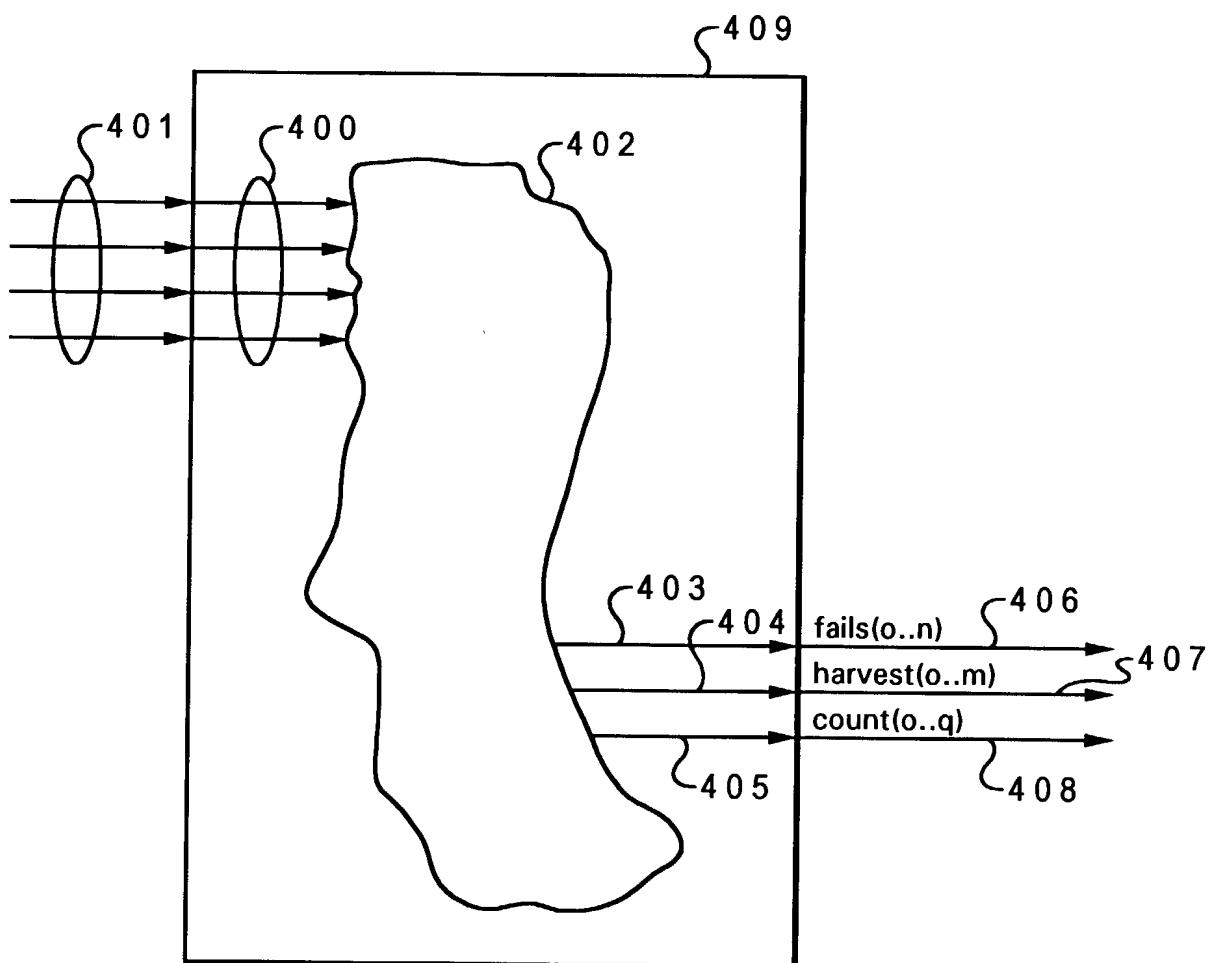


Fig. 4A

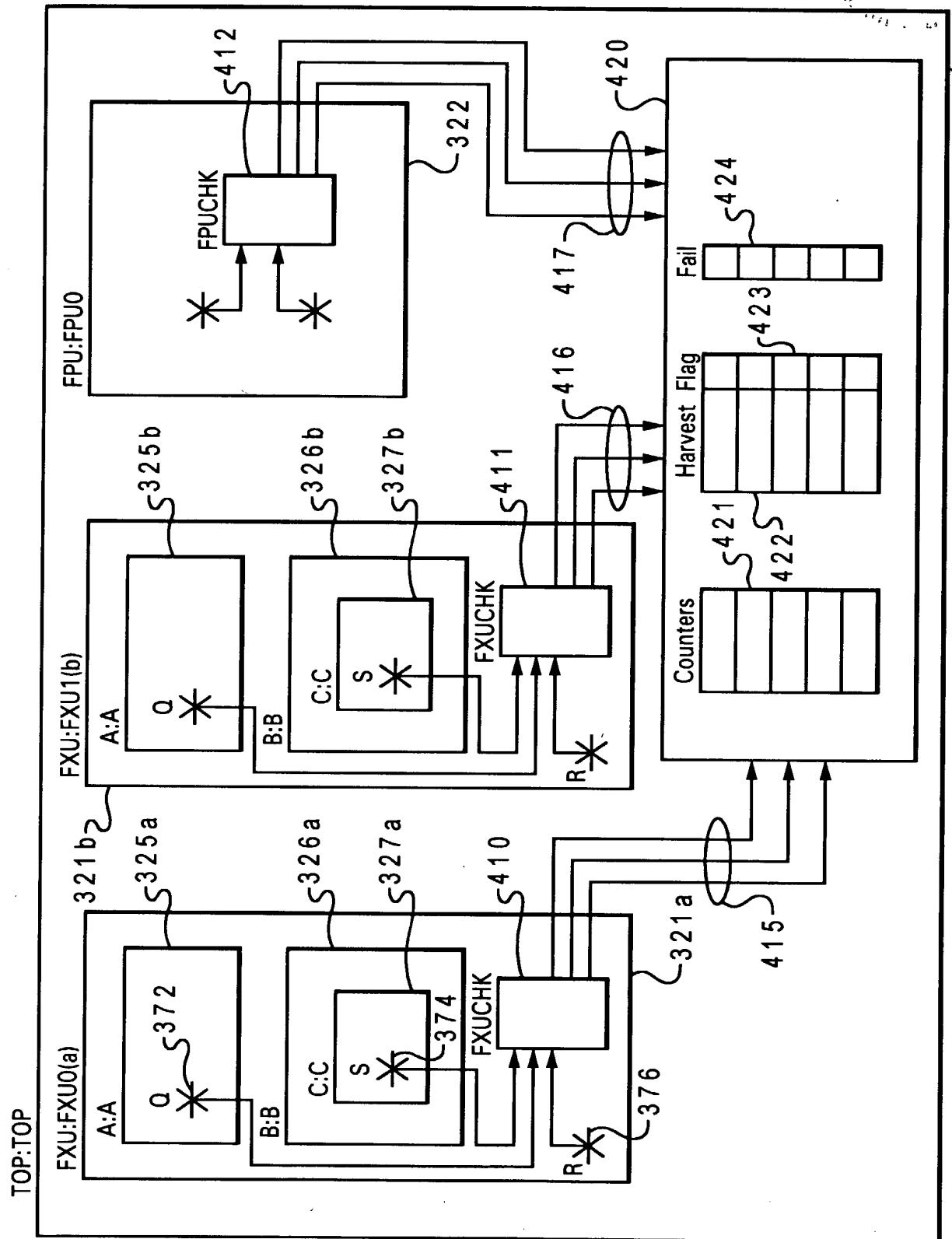


Fig. 4B

```

ENTITY FXUCHK IS
    PORT(
        S_IN      : IN std_ulogic;
        Q_IN      : IN std_ulogic;
        R_IN      : IN std_ulogic;
        clock     : IN std_ulogic;
        fails     : OUT std_ulogic_vector(0 to 1);
        counts    : OUT std_ulogic_vector(0 to 2);
        harvests  : OUT std_ulogic_vector(0 to 1);
    );

```

450

452 {--!! BEGIN
 --!! Design Entity: FXU;

453 {--!! Inputs
 --!! S_IN => B.C.S;
 --!! Q_IN => A.Q;
 --!! R_IN => R;
 --!! CLOCK => clock;
 --!! End Inputs

454 {--!! Fail Outputs;
 --!! 0 : "Fail message for failure event 0";
 --!! 1 : "Fail message for failure event 1";
 --!! End Fail Outputs;

440

455 {--!! Count Outputs;
 --!! 0 : <event0> clock;
 --!! 1 : <event1> clock;
 --!! 2 : <event2> clock;
 --!! End Count Outputs;

456 {--!! Harvest Outputs;
 --!! 0 : "Message for harvest event 0";
 --!! 1 : "Message for harvest event 1";
 --!! End Harvest Outputs;

457 {--!! End;

451

ARCHITECTURE example of FXUCHK IS

BEGIN

458

... HDL code for entity body section ...

END;

Fig. 4C

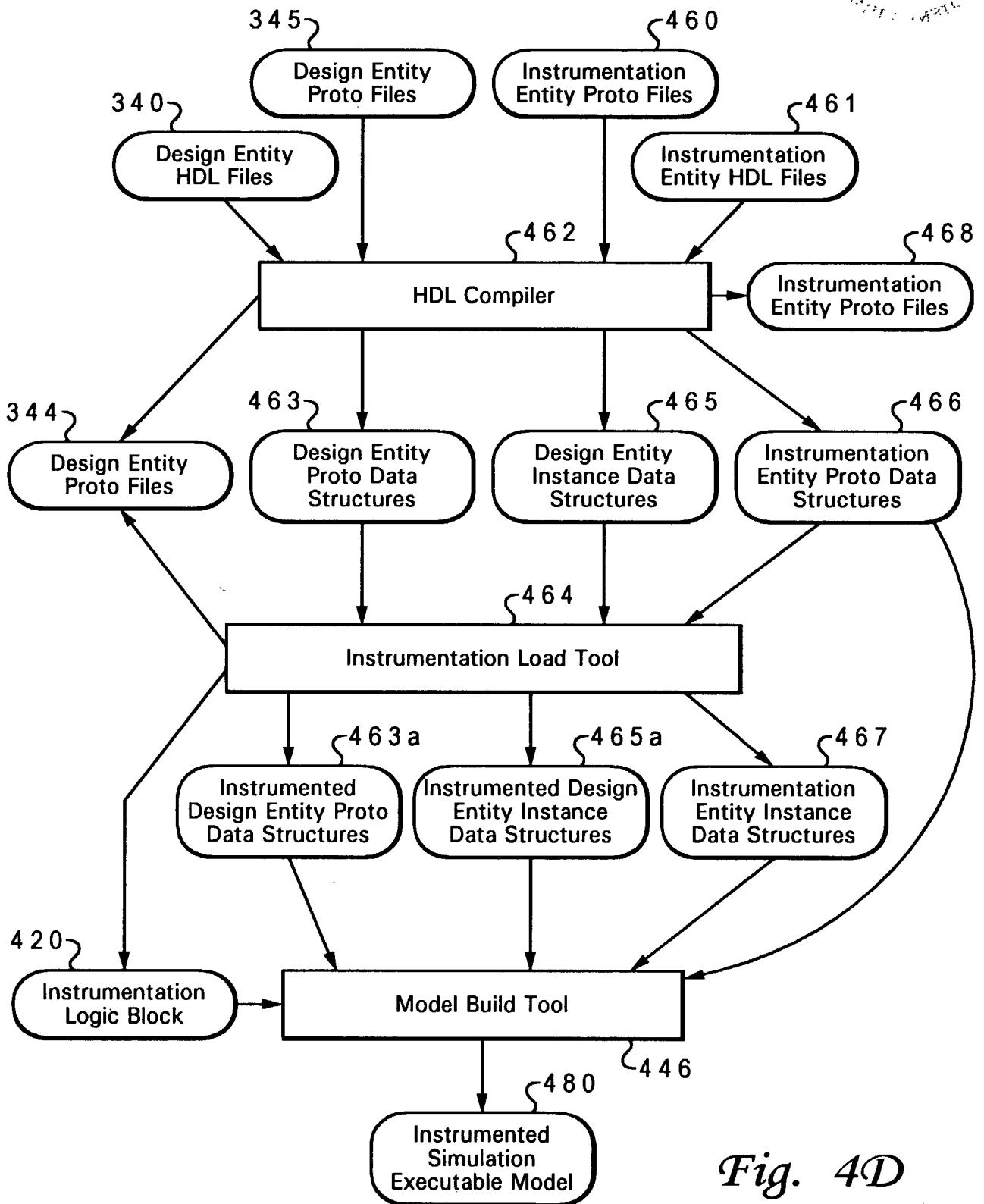


Fig. 4D

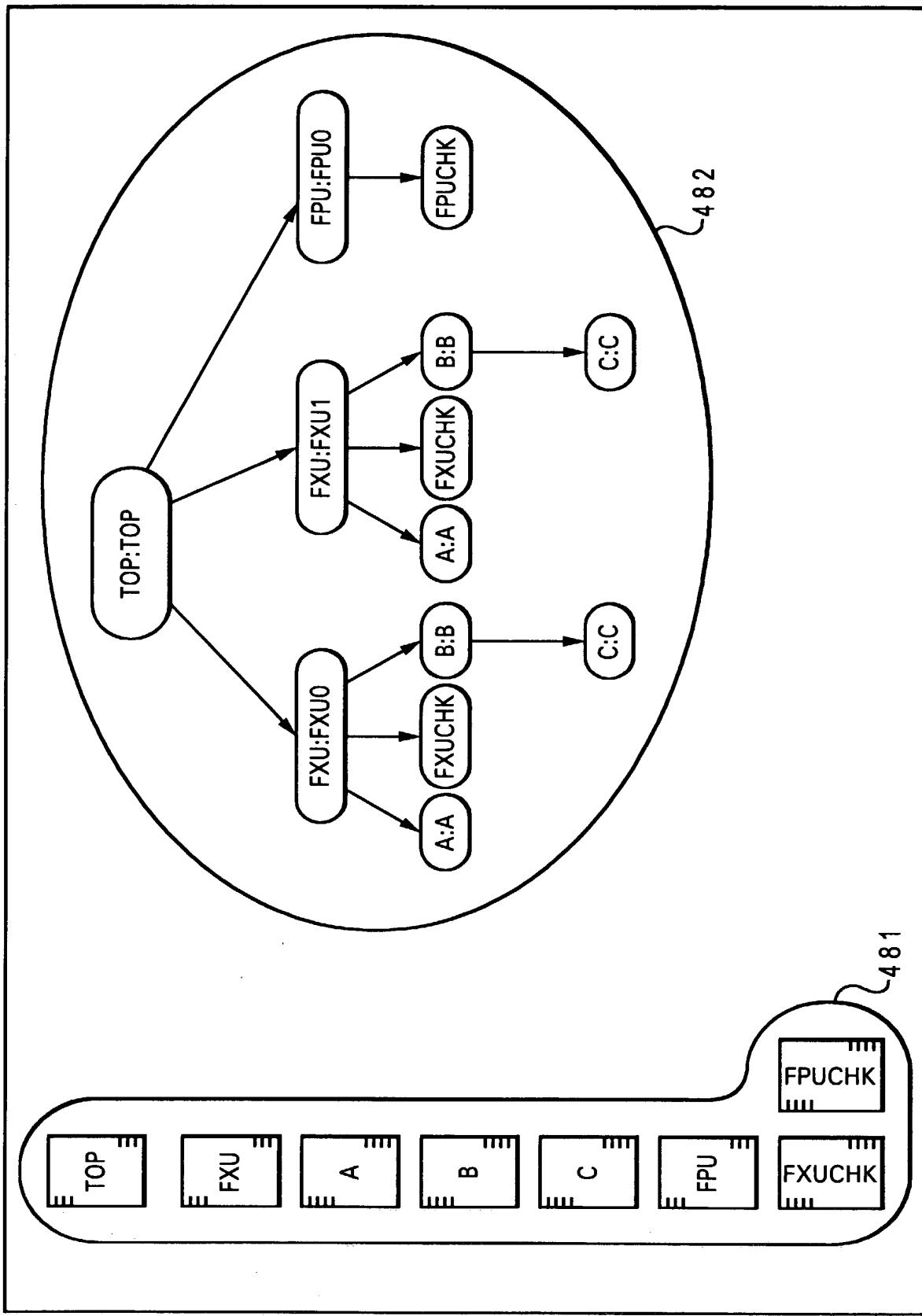


Fig. 4E

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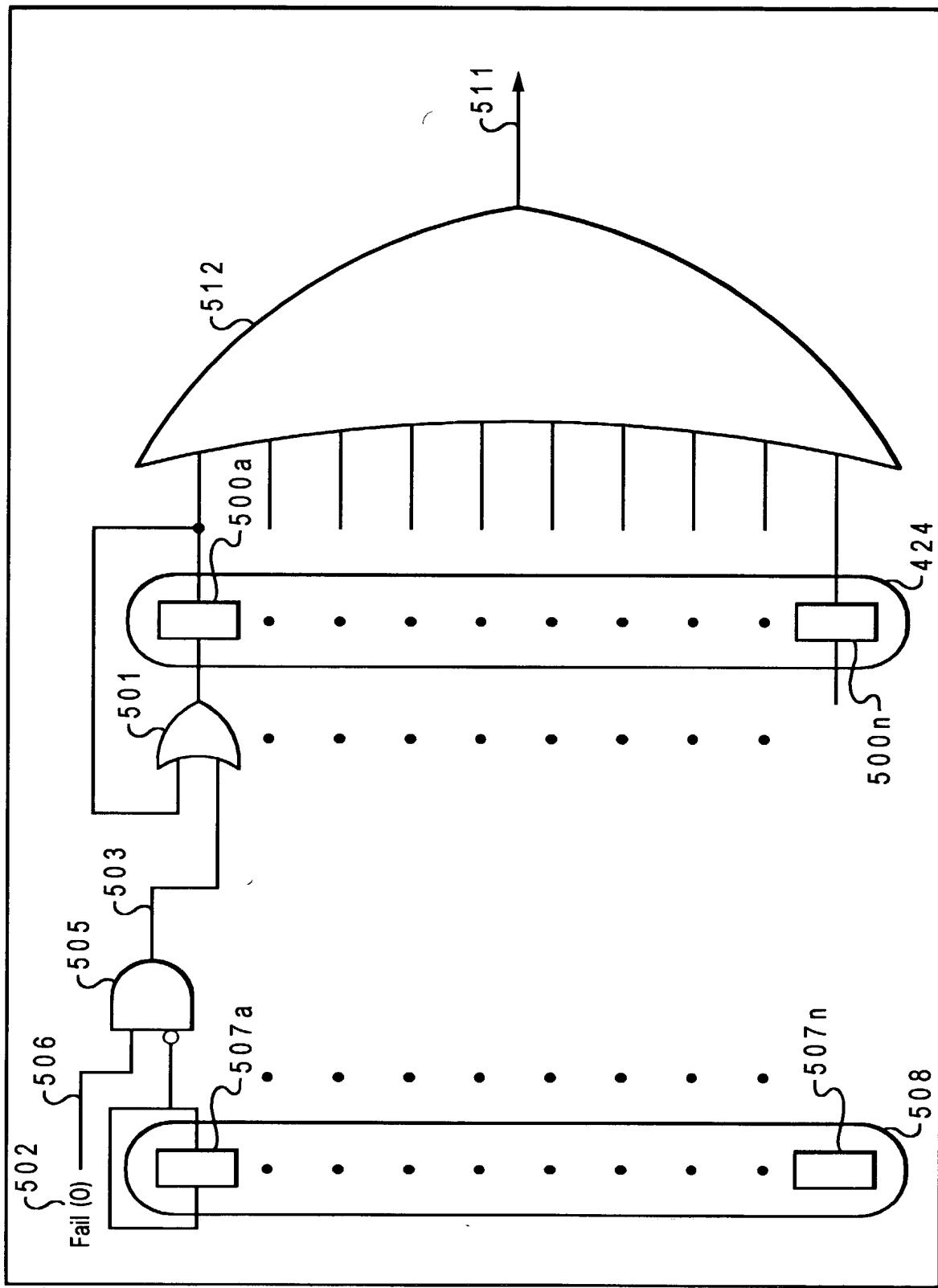


Fig. 5A

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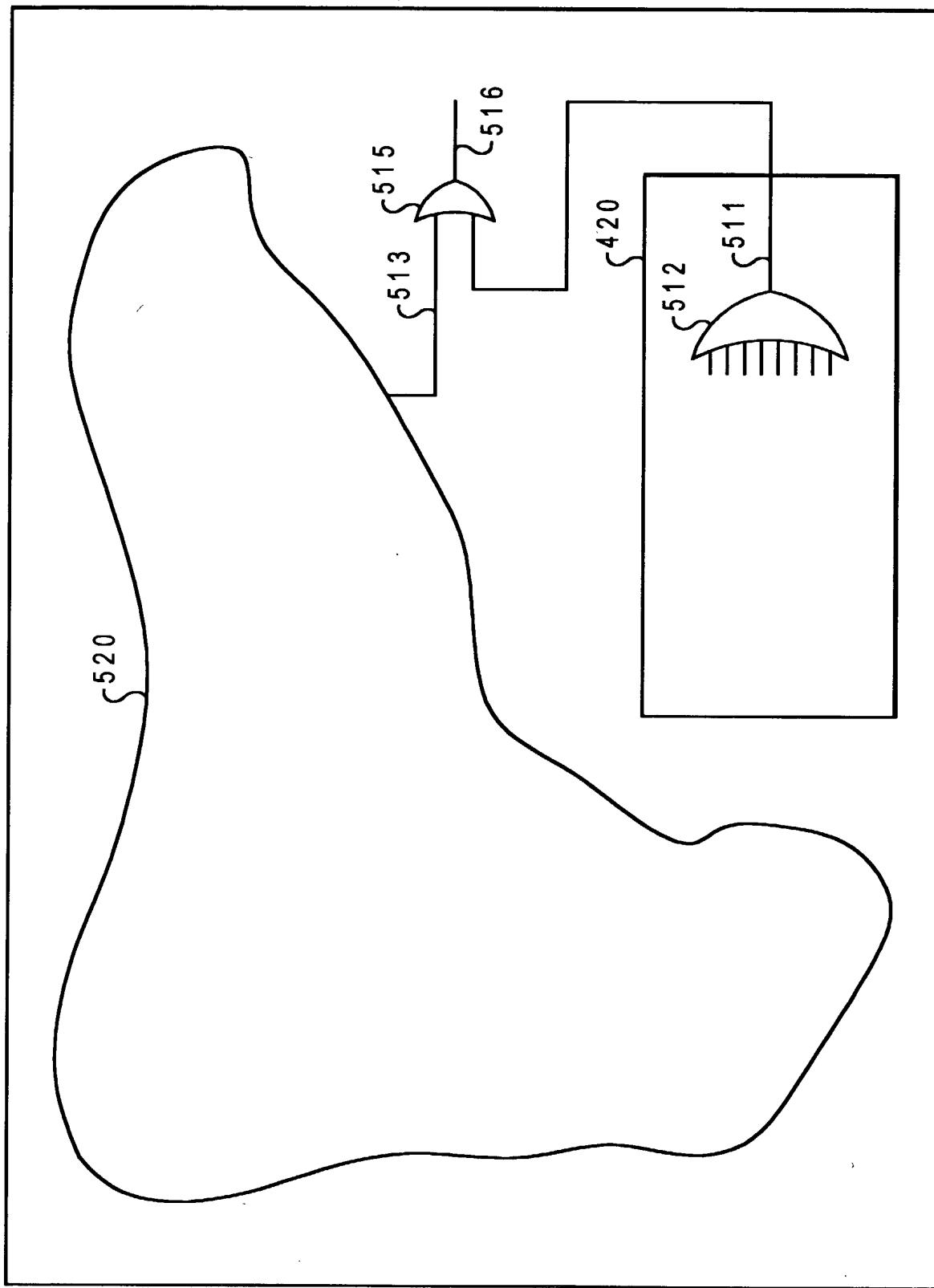


Fig. 5B

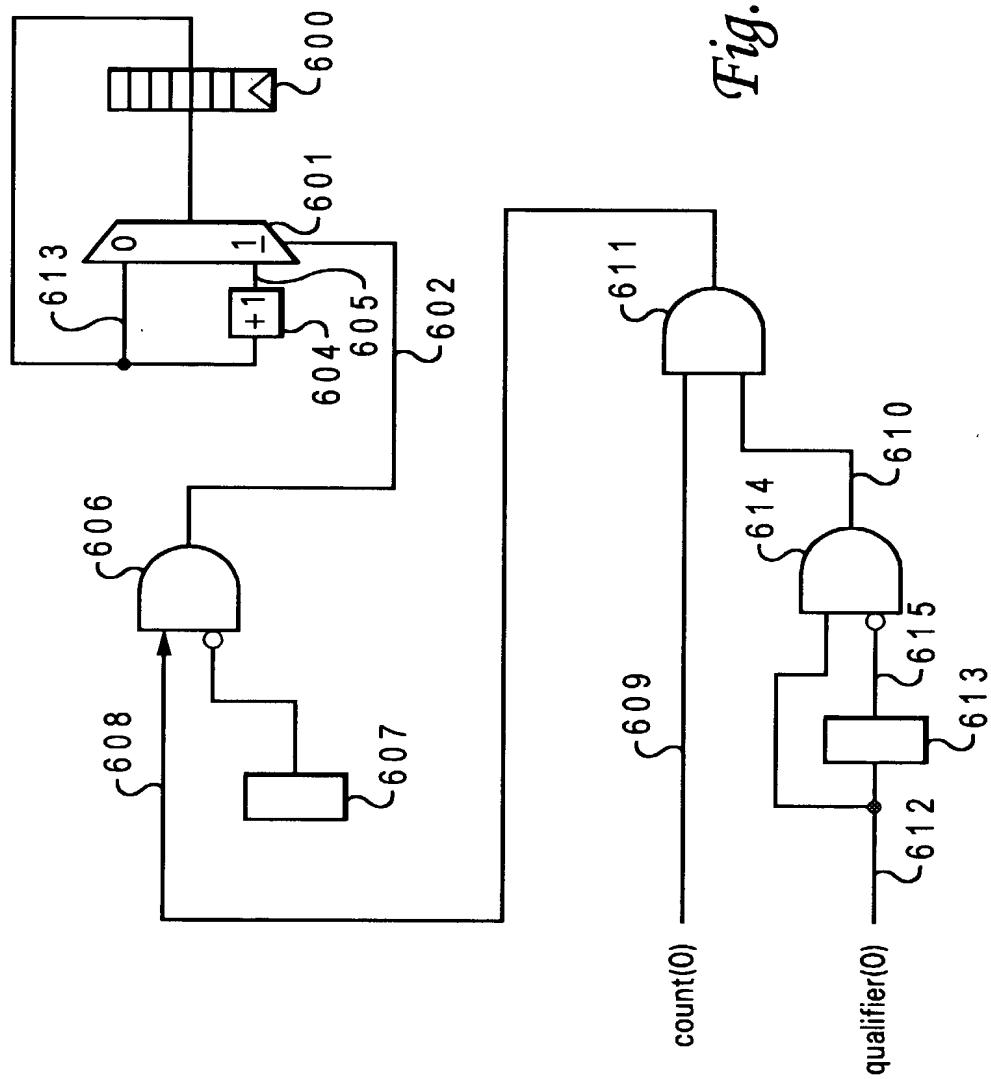


Fig. 6A

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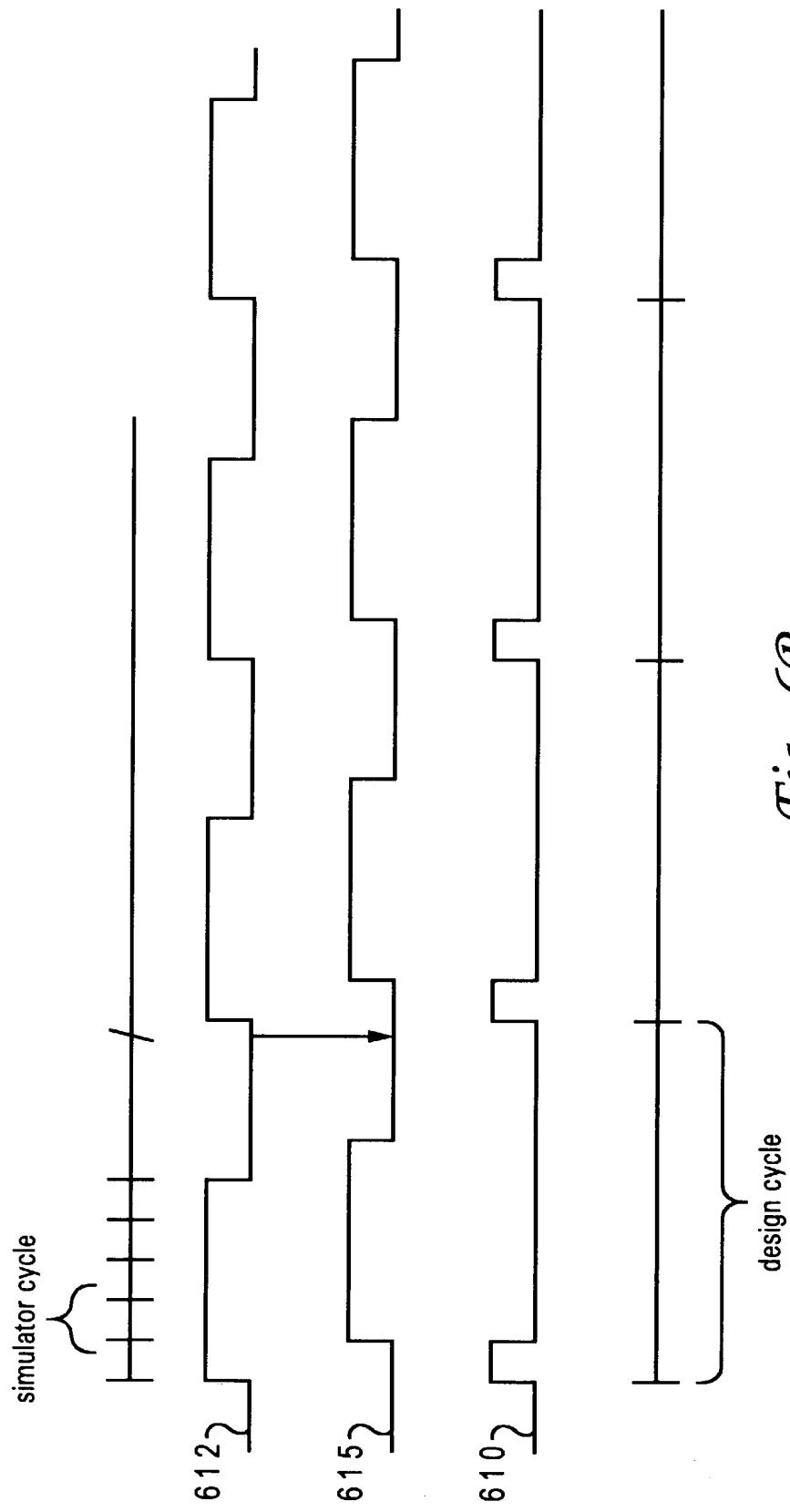


Fig. 6B

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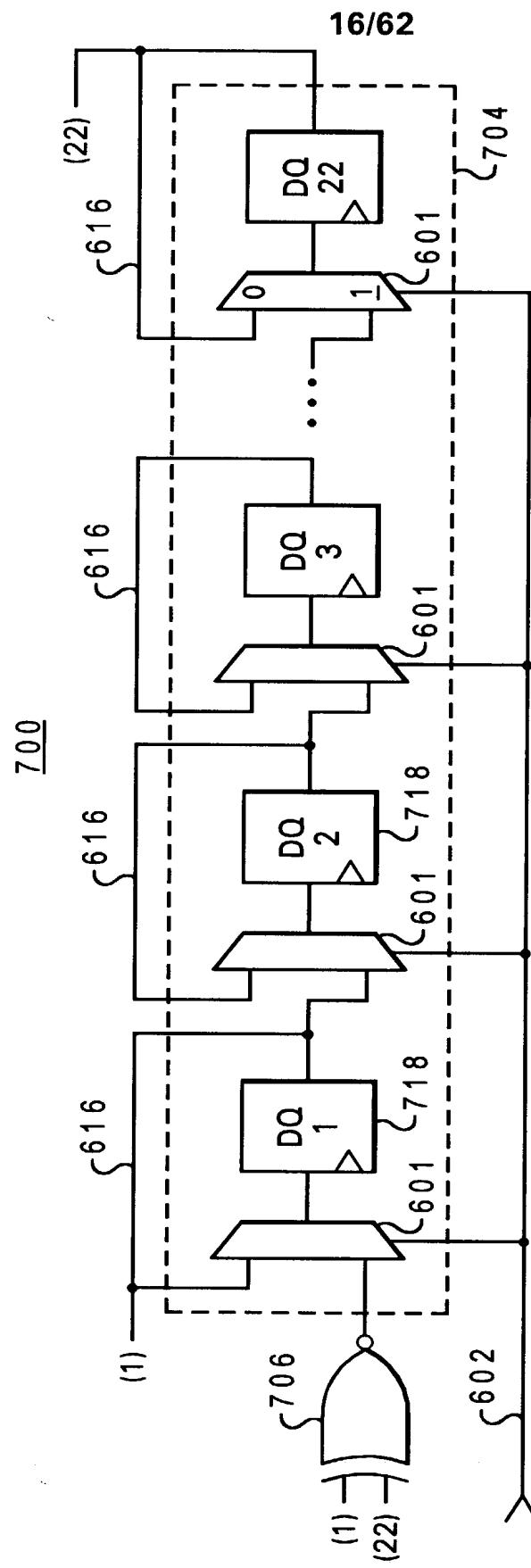


Fig. 7

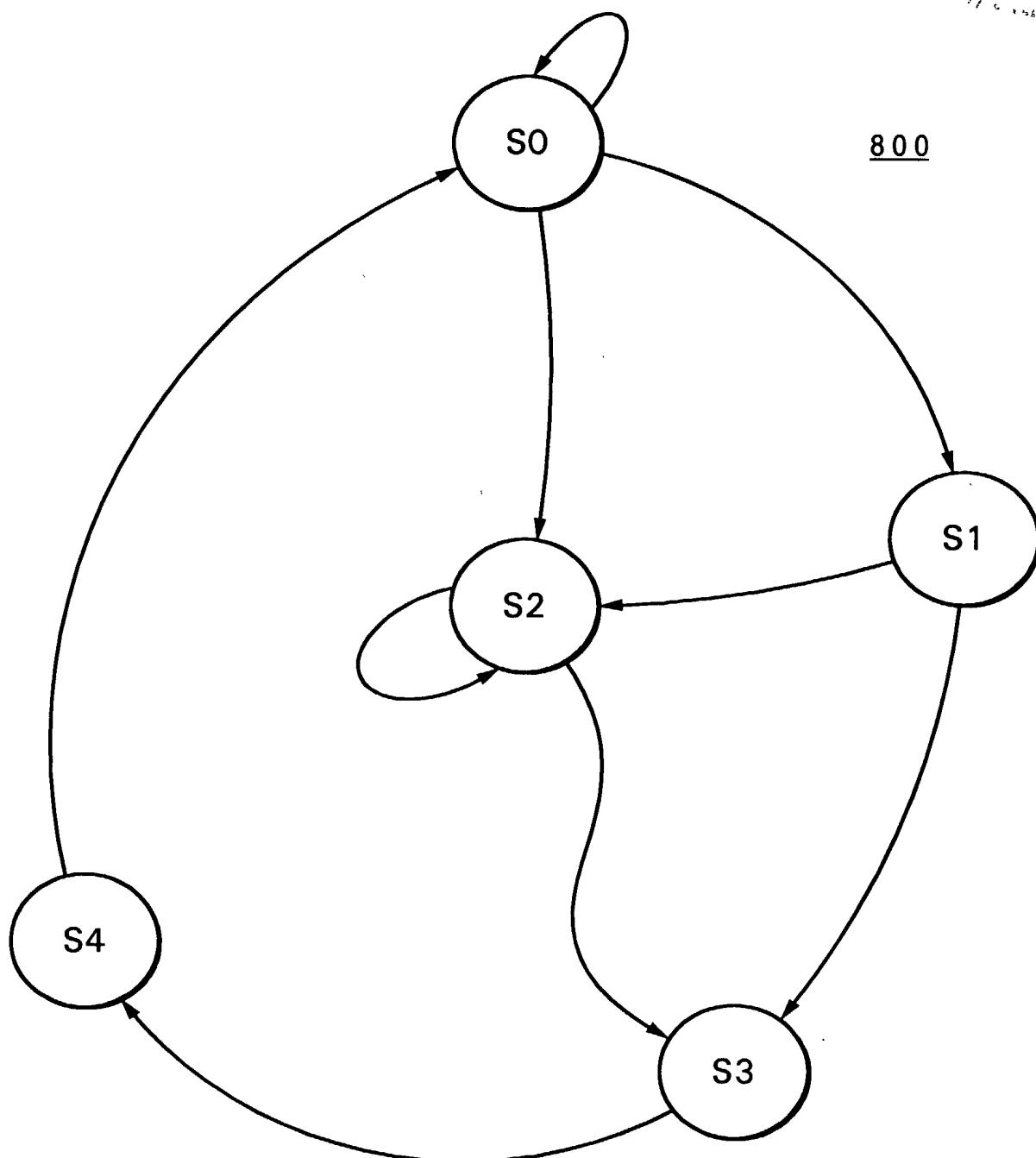


Fig. 8A
Prior Art

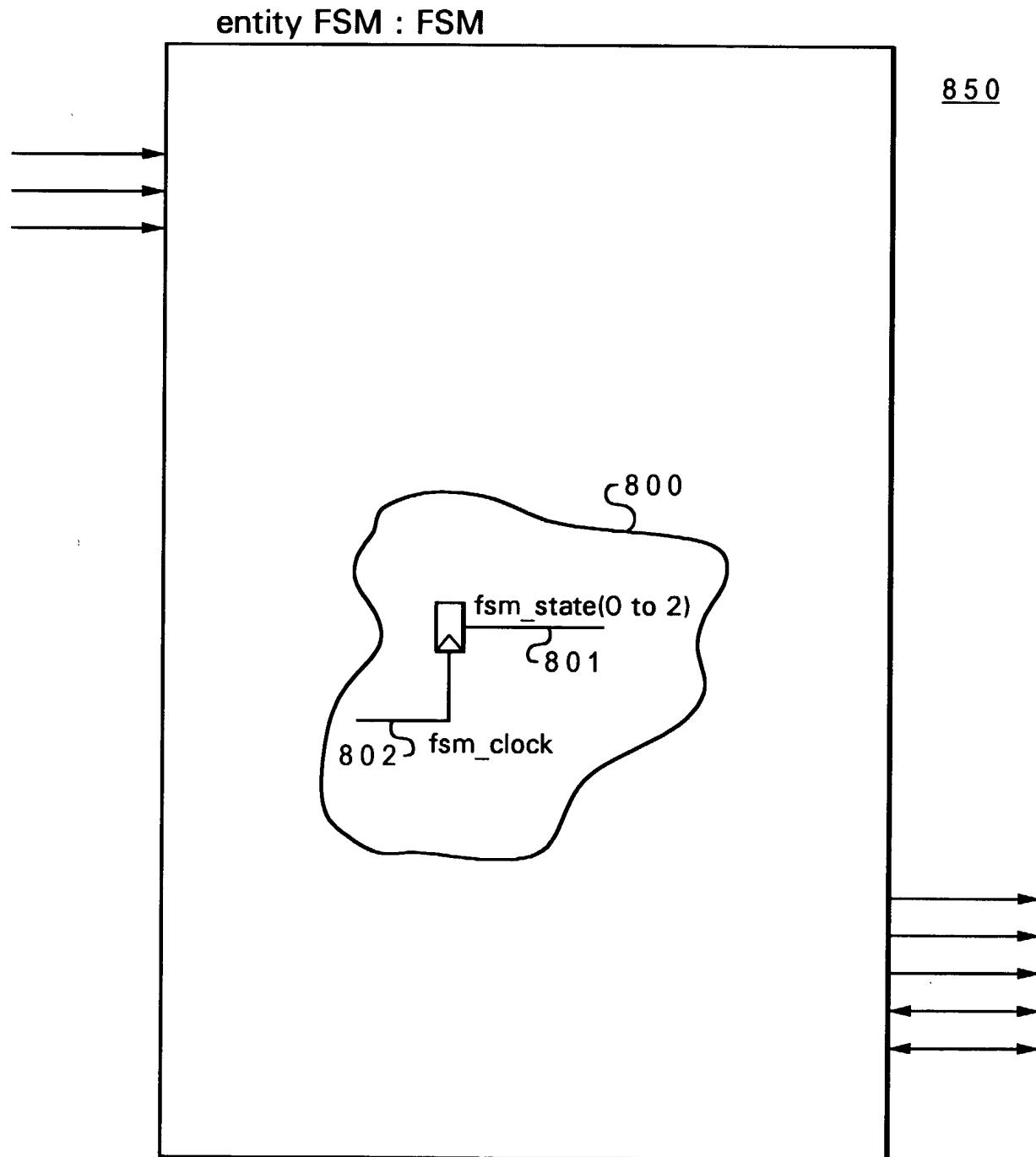


Fig. 8B
Prior Art

ENTITY FSM IS

```
PORT(  
      ....ports for entity fsm....  
);
```

ARCHITECTURE FSM OF FSM IS

BEGIN

... HDL code for FSM and rest of the entity ...

fsm_state(0 to 2) <= ... Signal 801 ...

```
853 { --!! Embedded FSM : examplefsm;  
859 { --!! clock          : (fsm_clock);  
854 { --!! state_vector   : (fsm_state(0 to 2));  
855 { --!! states         : (S0, S1, S2, S3, S4);  
856 { --!! state_encoding : ('000', '001', '010', '011', '100');  
     { --!! arcs          : (S0 => S0, S0 => S1, S0 => S2,  
     { --!!                  (S1 => S2, S1 => S3, S2 => S2,  
     { --!!                  (S2 => S3, S3 => S4, S4 => S0);  
858 { --!! End FSM;
```

END;

Fig. 8C

entity FSM : FSM

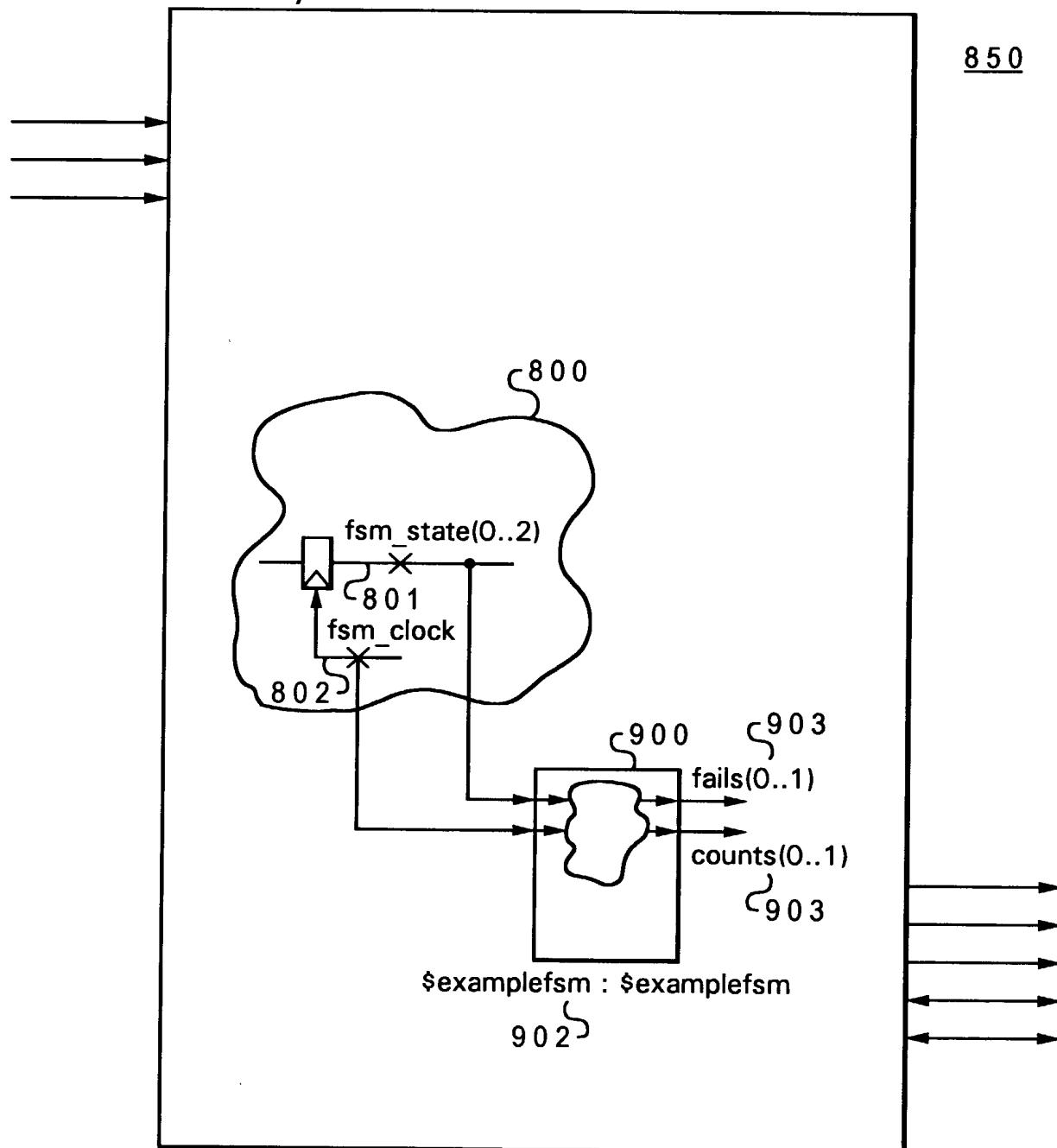
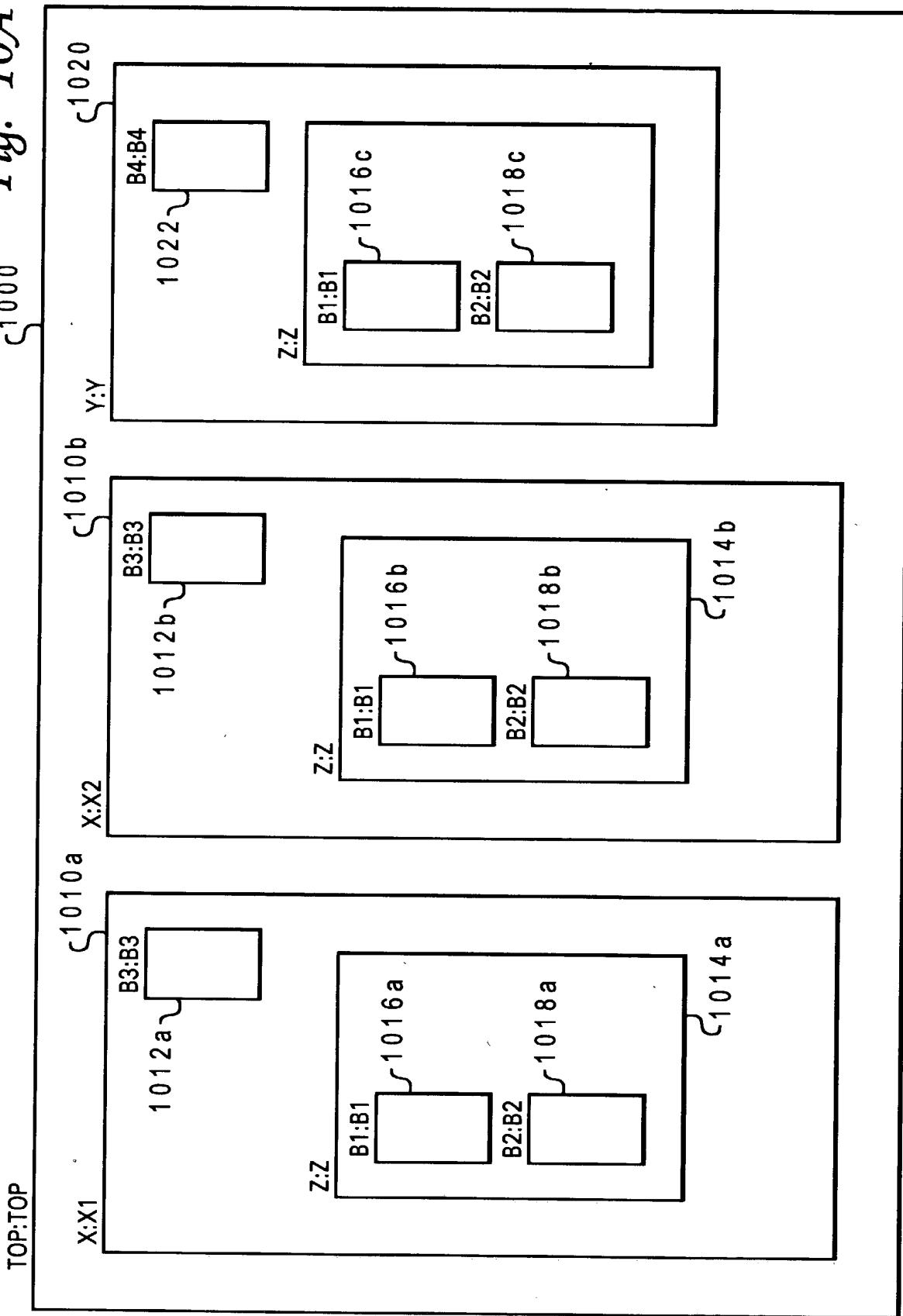


Fig. 9

Fig. 10A



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1030 1032 1034 1036
<instantiation identifier>.<instrumentation entity name>.<design entity name>.<eventname>

Fig. 10B

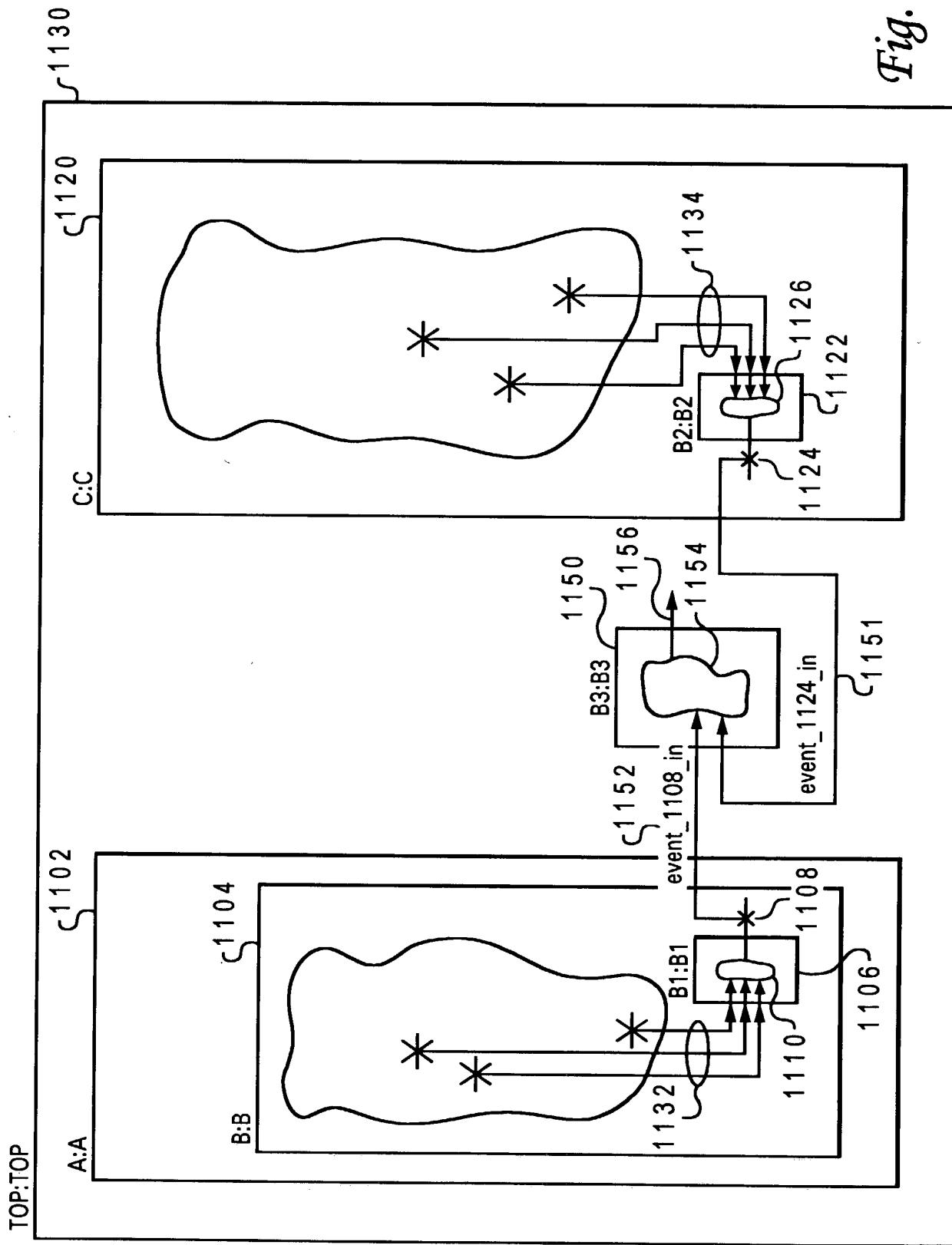
X1	B3	X	1040
X1.Z	B1	Z	1041
X1.Z	B2	Z	1042
X2	B3	X	1043
X2.Z	B1	Z	1044
X2.Z	B2	Z	1045
Y	B4	Y	1046
Y.Z	B1	Z	1047
Y.Z	B2	Z	1048
			COUNT1

Fig. 10C

1030 1034 1036
<instantiation identifier>.<design entity name>.<eventname>

Fig. 10D

Fig. 11A



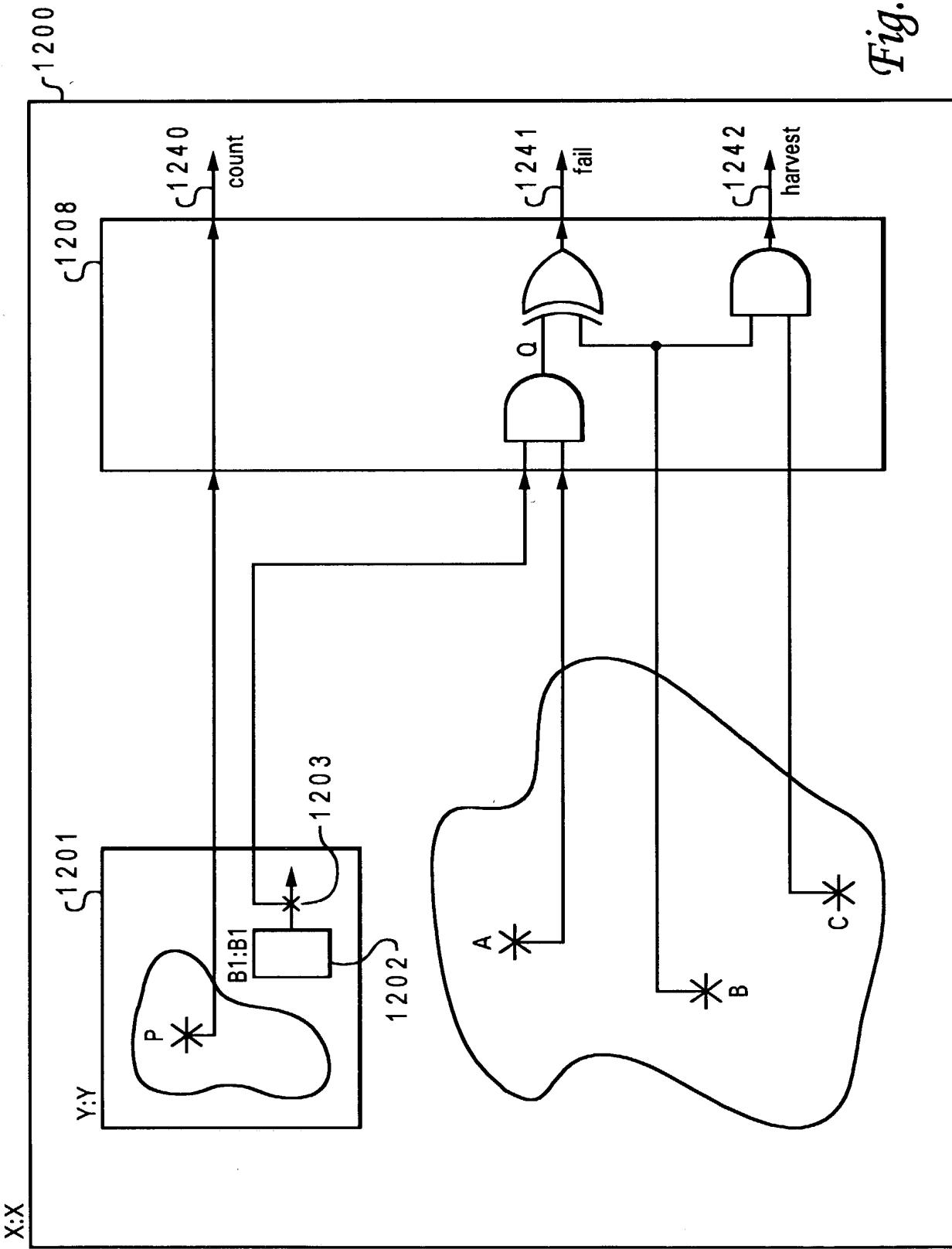
```
--!! Inputs  
--!! event_1108_in <= C.[B2.count.event_1108];  
--!! event_1124_in <= A.B.[B1.count.event_1124];  
--!! End Inputs
```

1163 1165 1161
1164 1166 1162

Fig. 11B

```
--!! Inputs
--!! event_1108_in <= C.[count.event_1108]; 1171
--!! event_1124_in <= B.[count.event_1124]; 1172
--!! End Inputs
```

Fig. 11C



ENTITY X IS

```
PORT( :  
      :  
      );
```

ARCHITECTURE example of X IS

BEGIN

... HDL code for X ...

1220

1221 {
 Y:Y
 PORT MAP(:
 :
);

1222 {
 A <=
 B <=
 C <=

1223 {
 --!! [count, countname0, clock] <= Y.P;
 --!! Q <= Y. [B1.count.count1] AND A;
 --!! [fail, failname0, "fail.msg"] <= Q XOR B;
 --!! [harvest, harvestname0, "harvest msg"] <= B AND C;

END;

1230

1232

1234

1236

Fig. 12B

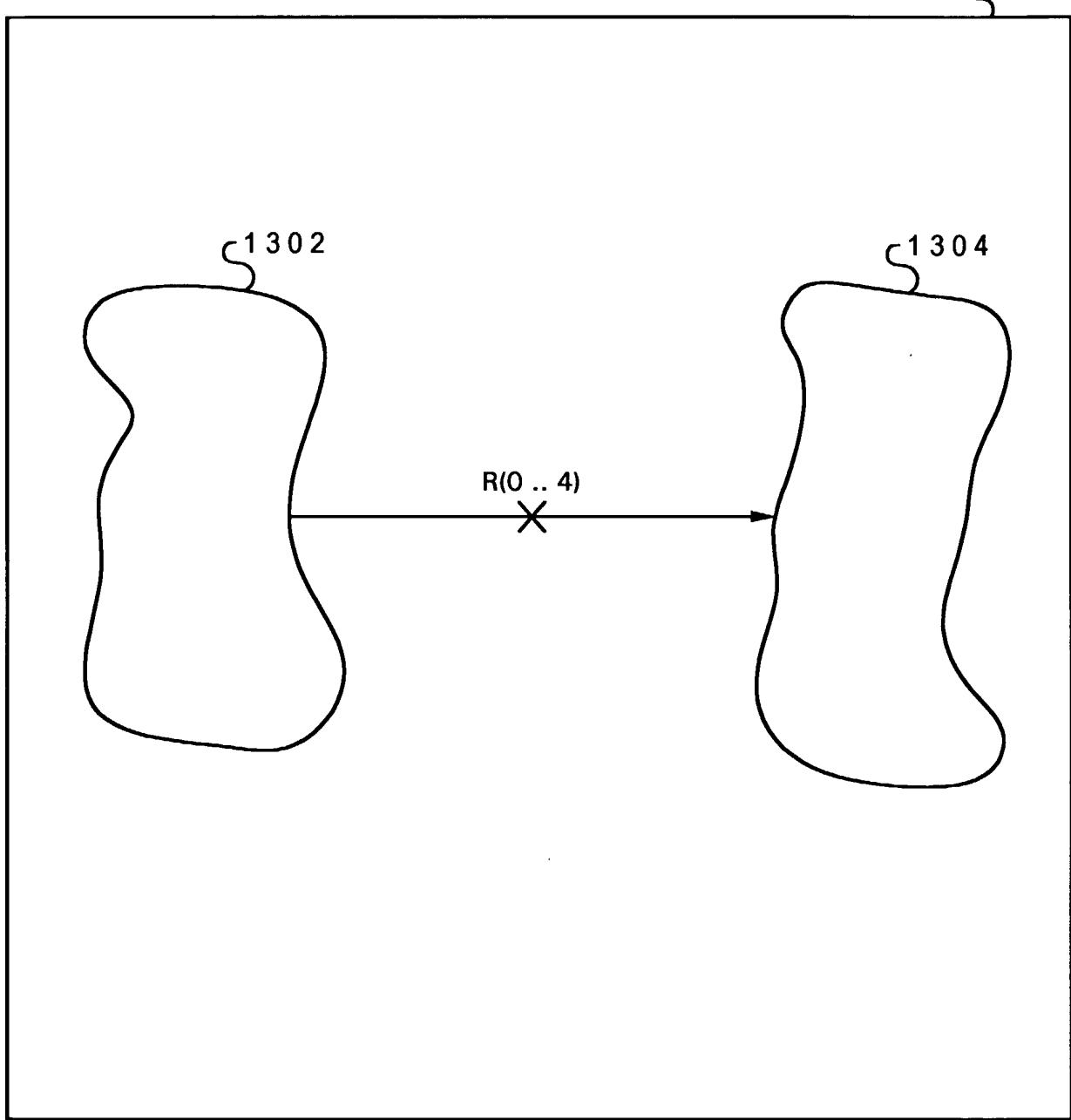


Fig. 13A

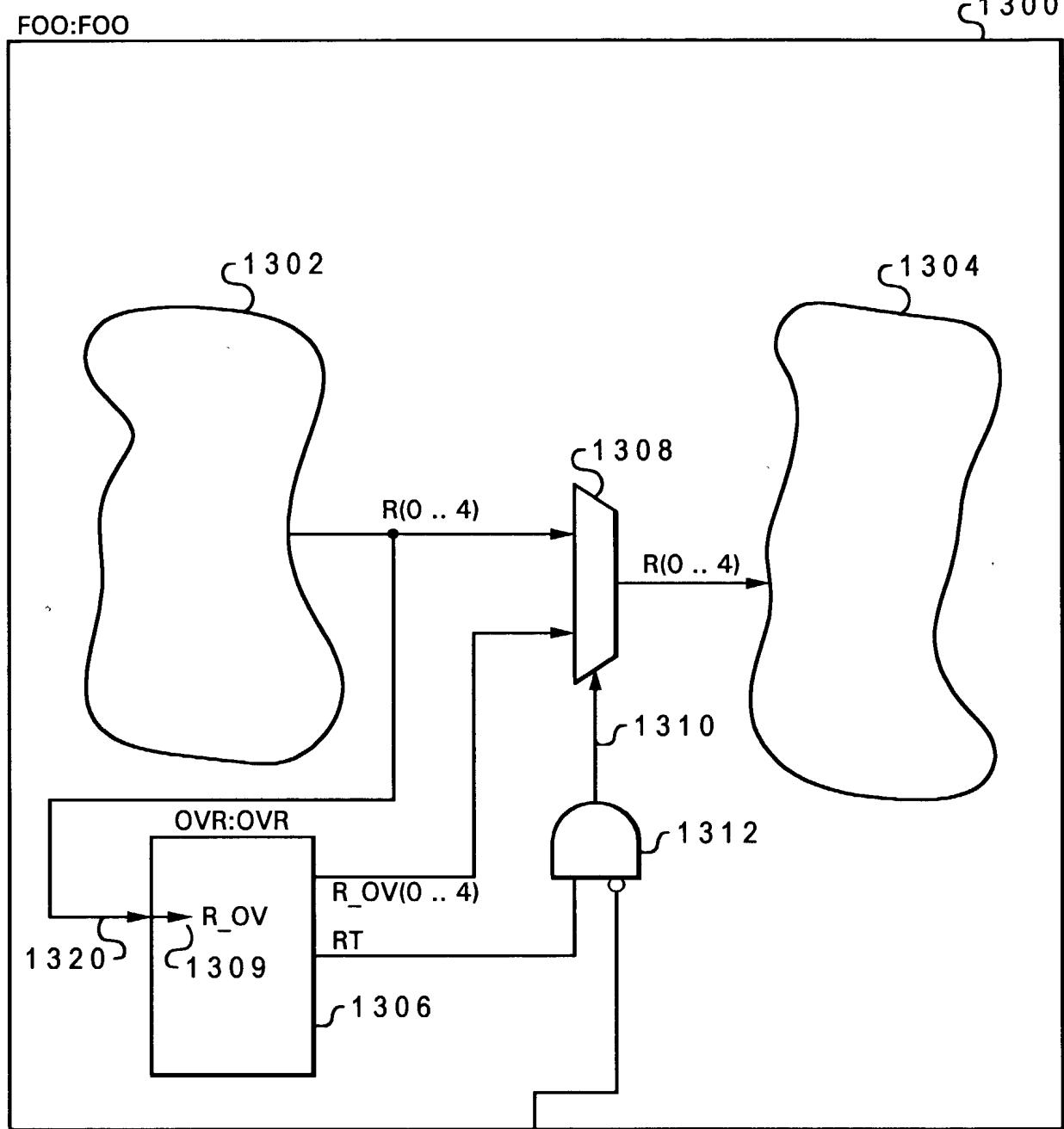


Fig. 13B

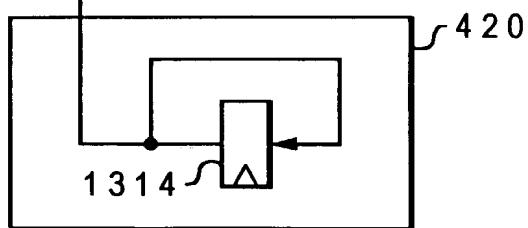


Fig. 13C

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ENTITY FOO IS

```
PORT( :  
      :  
      :  
      );
```

ARCHITECTURE example of FOO IS

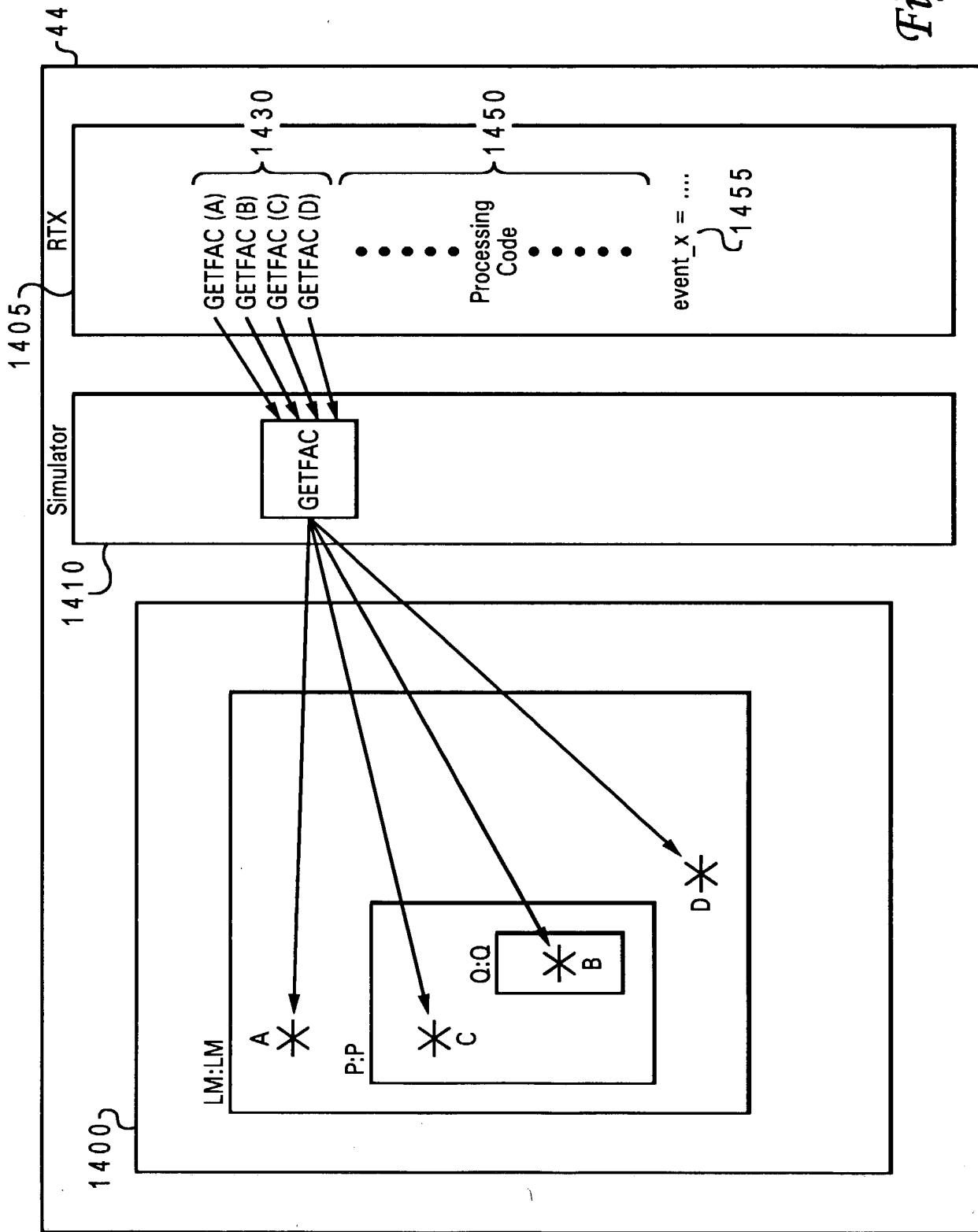
BEGIN

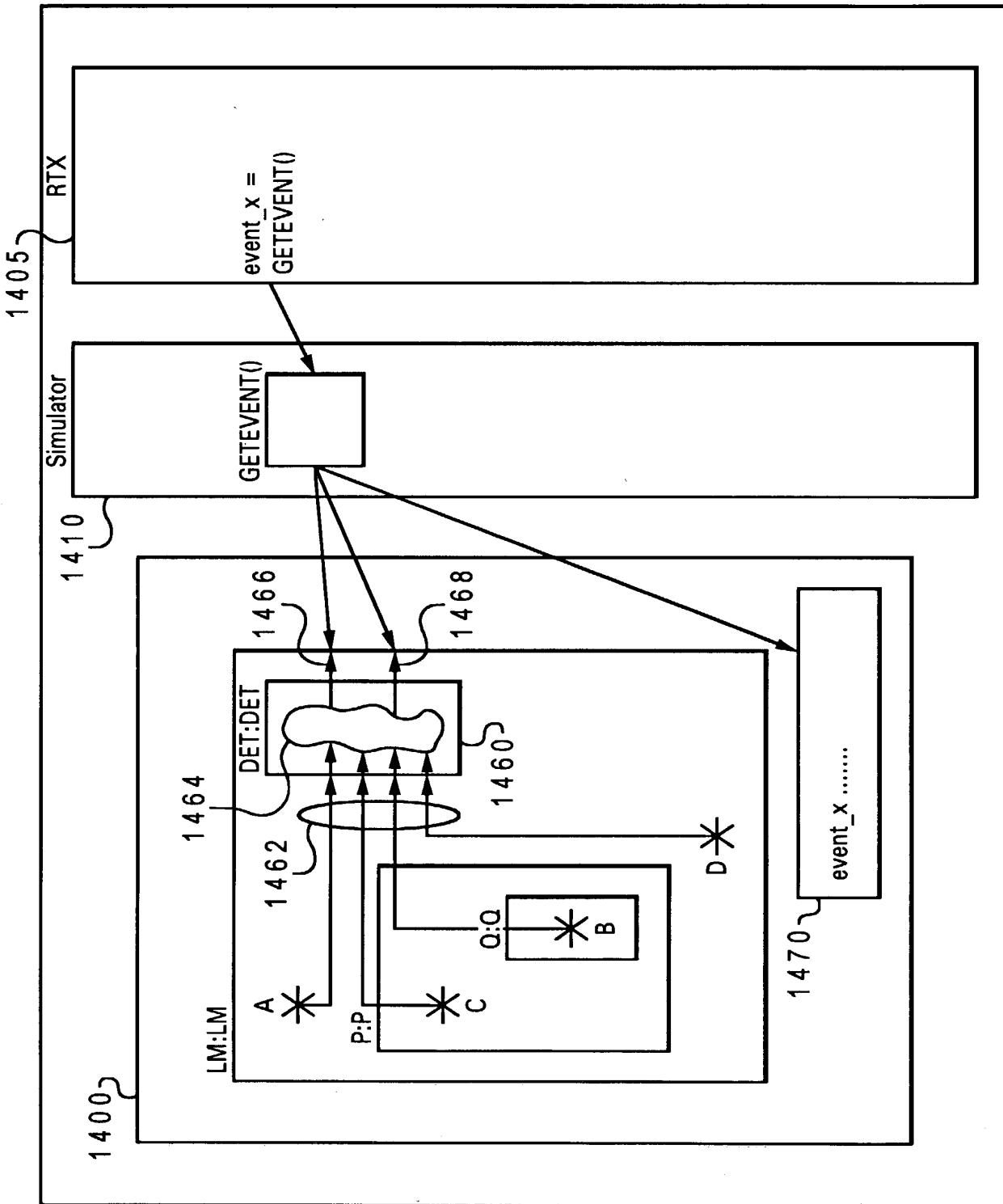
```
  .  
  .  
  .  
  .  
  R <= .....  
  .  
  .  
  .  
  .
```

1380 {
 --!! R_IN <= {R};
 --!! R_OV(0 to 4) <=; 1383
 --!! RT <=;
 --!! [override, R_OVERRIDE, R(0 .. 4), RT] <= R_OV(0 to 4);
 } 1384

Fig. 13D

Fig. 14A





ENTITY DET IS

```

PORT( A      : IN std_ulogic;
      B      : IN std_ulogic_vector(0 to 5);
      C      : IN std_ulogic;
      D      : IN std_ulogic;
      ...
      event_x : OUT std_ulogic_vector(0 to 2);
      x_here  : OUT std_ulogic;
);

--!! BEGIN
--!! Design Entity: LM;
--!! Inputs
--!! A      => A;
--!! B      => P.Q.B;
--!! C      => P.C;
--!! D      => D;
--!! End Inputs
--!! Detections
--!! <event_x>:event_x(0 to 2) [x_here];
--!! End Detections
--!! End;
--!! End;

1491 {1493
1494 }1495
1492 {1496
1497 }1498
    
```

1480

1491 } 1493

1494 } 1495

1492 } 1496

1497 } 1498

Fig. 14C

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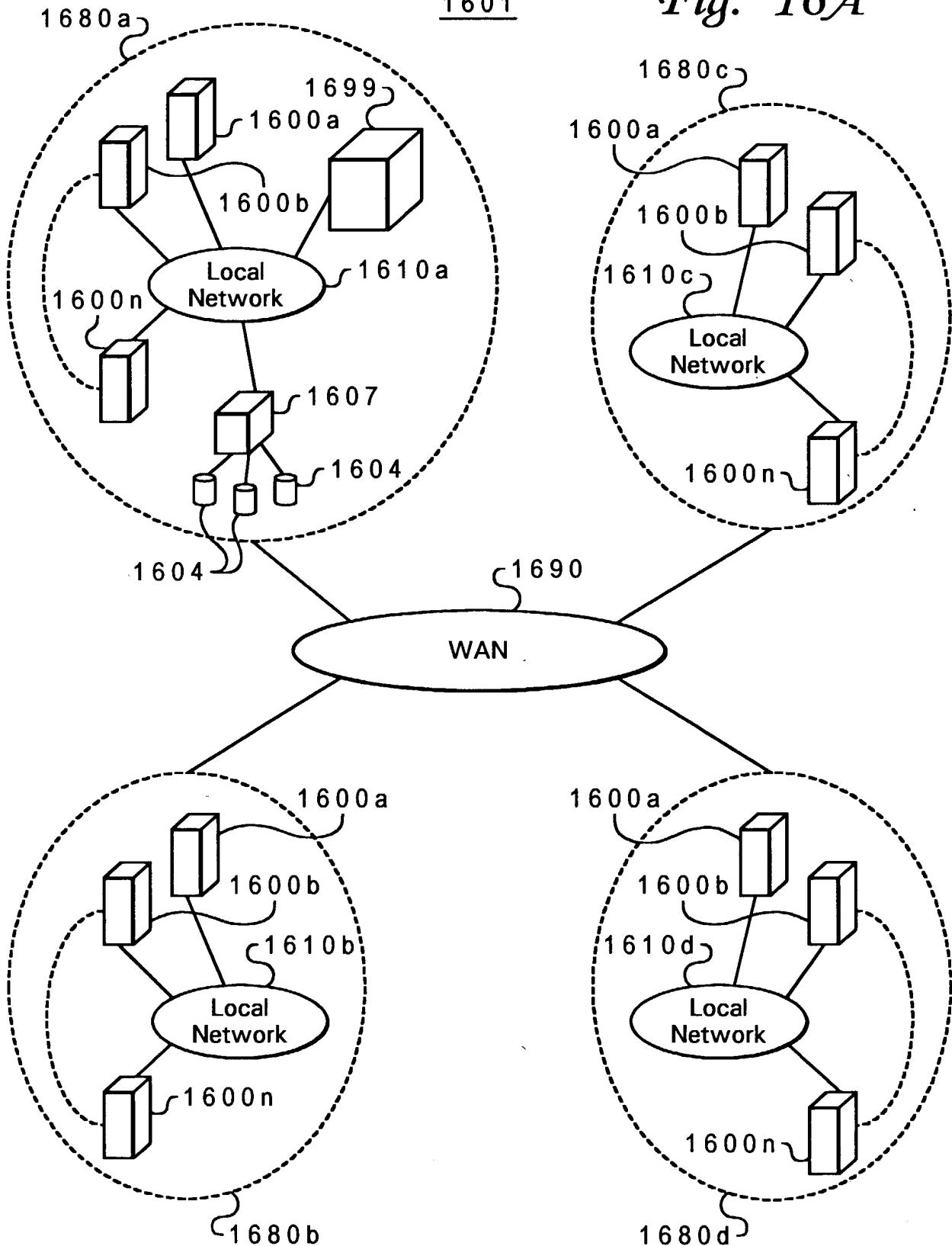
1660

	1661	1662		
1663	1: X1	B3	X	COUNT1
	2: X1.Z	B1	Z	COUNT1
	3: X1.Z	B2	Z	COUNT1
	4: X2	B3	X	COUNT1
	5: X2.Z	B1	Z	COUNT1
	6: X2.Z	B2	Z	COUNT1
	7: Y	B4	Y	COUNT1
	8: Y.Z	B1	Z	COUNT1
	9: Y.Z	B2	Z	COUNT1

Fig. 15

1601

Fig. 16A



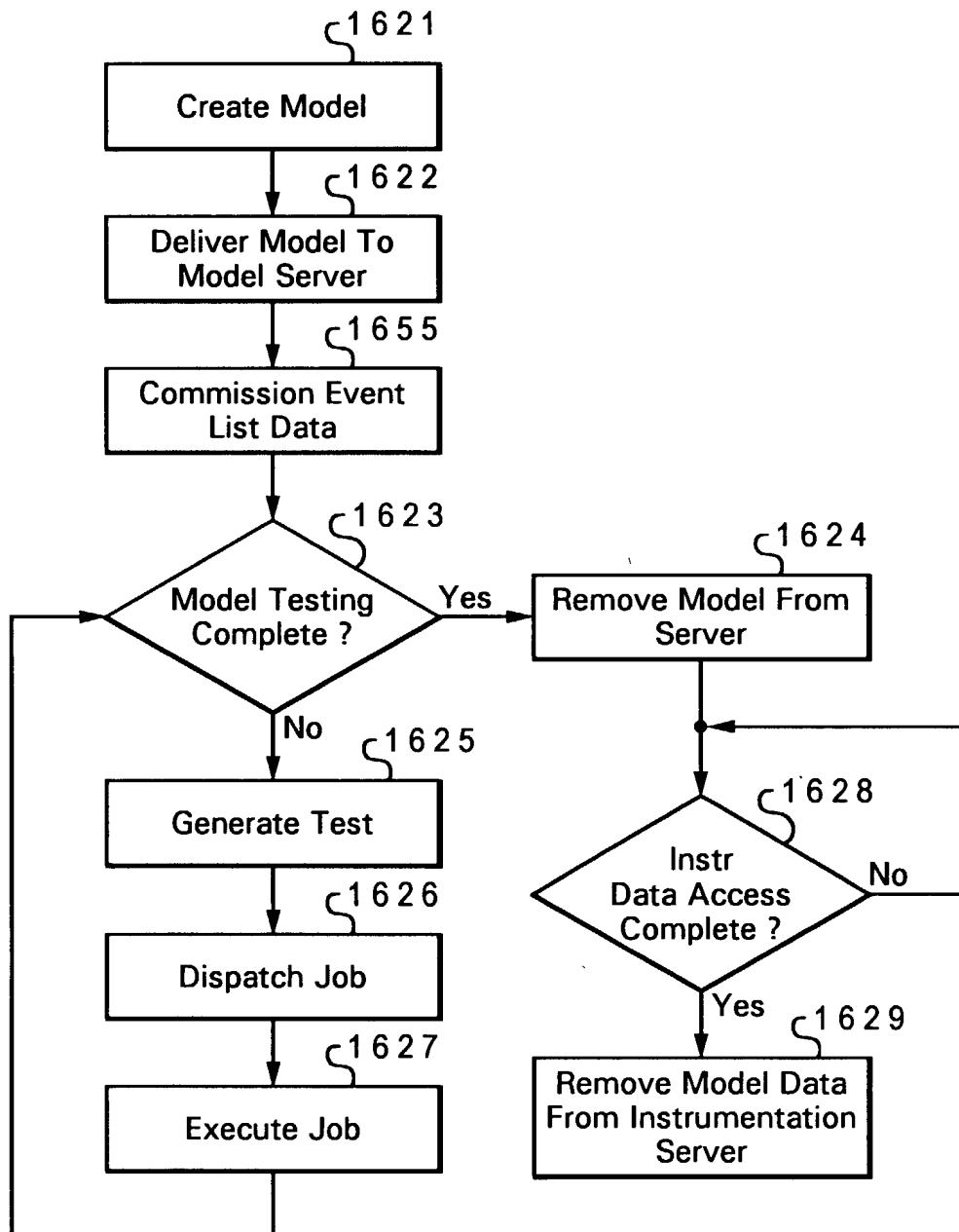


Fig. 16B

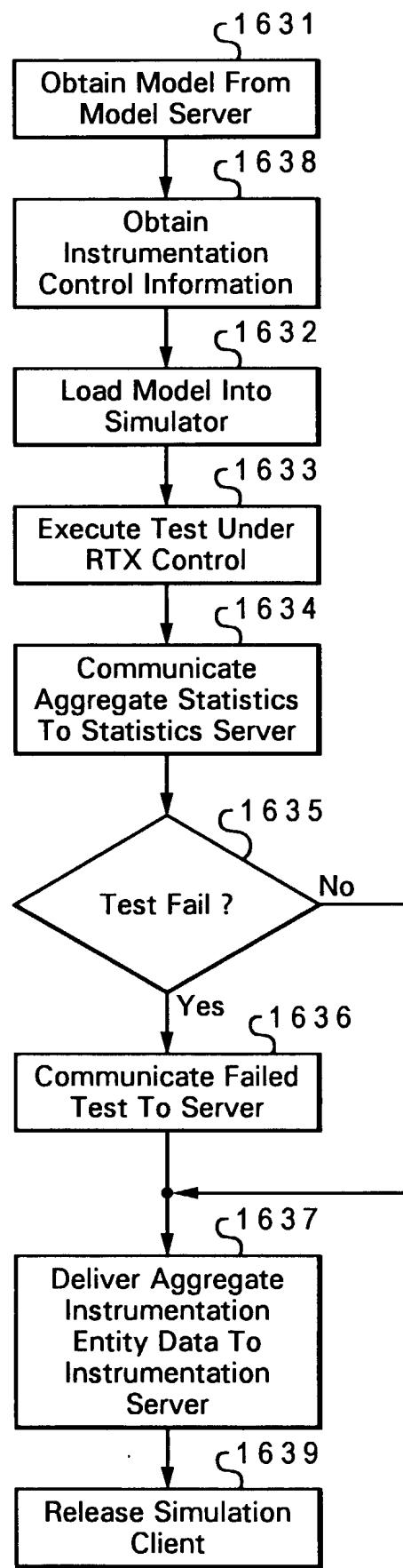


Fig. 16C

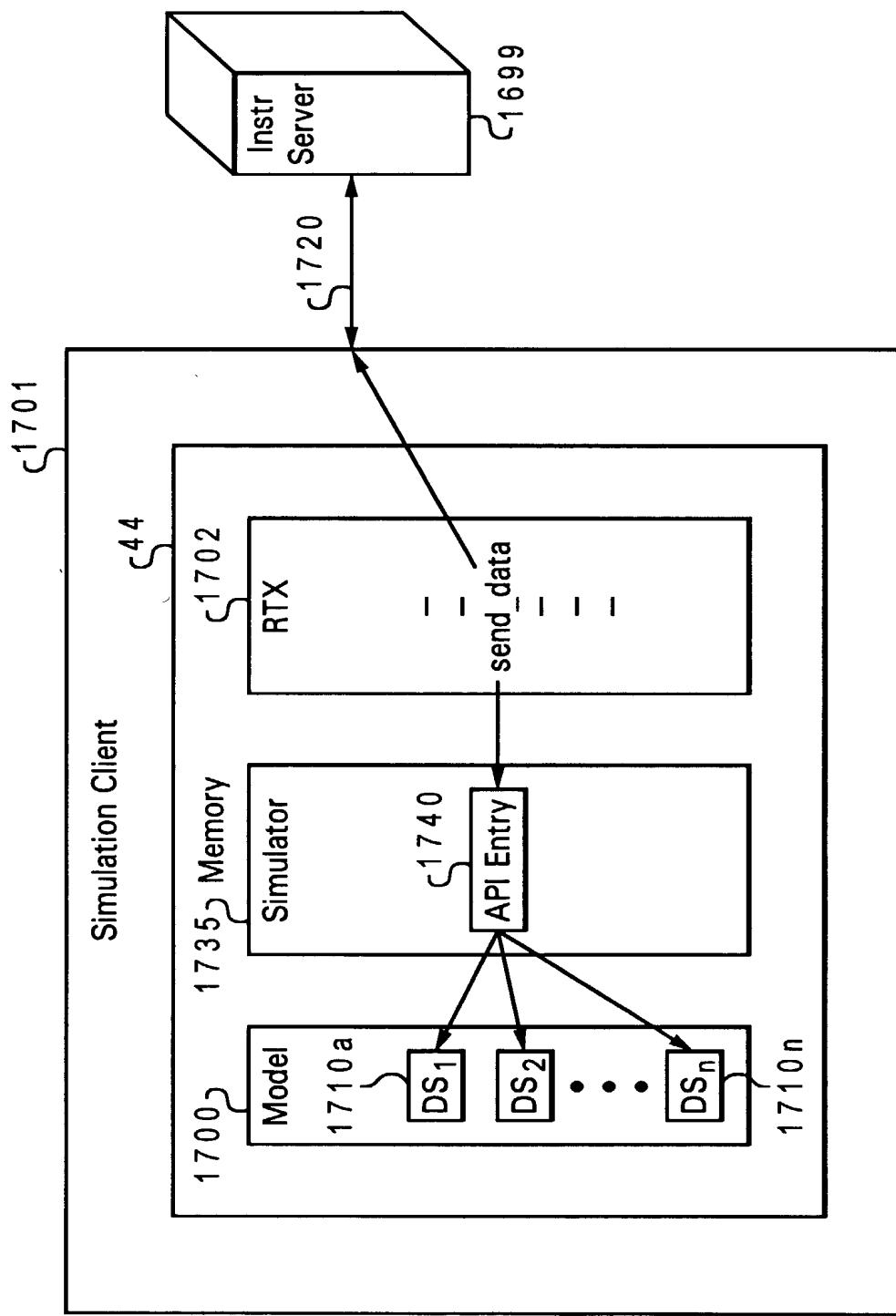


Fig. 17A

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1750

1751

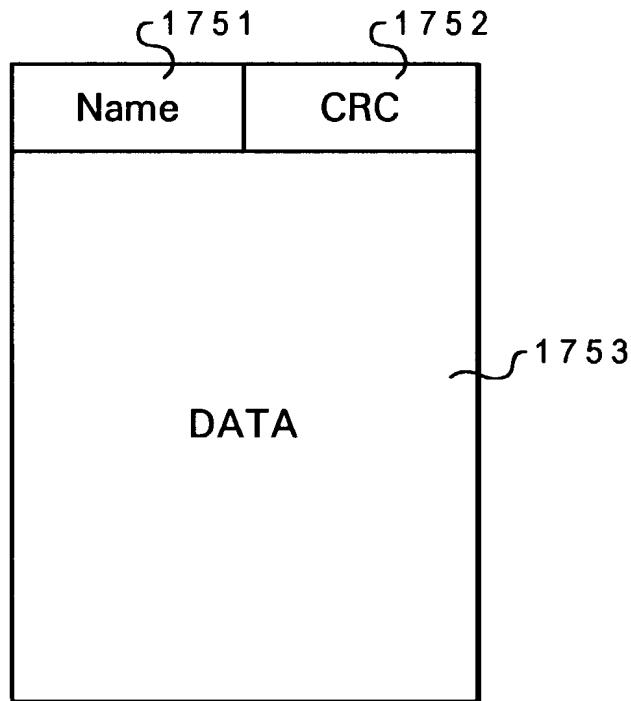


Fig. 17B

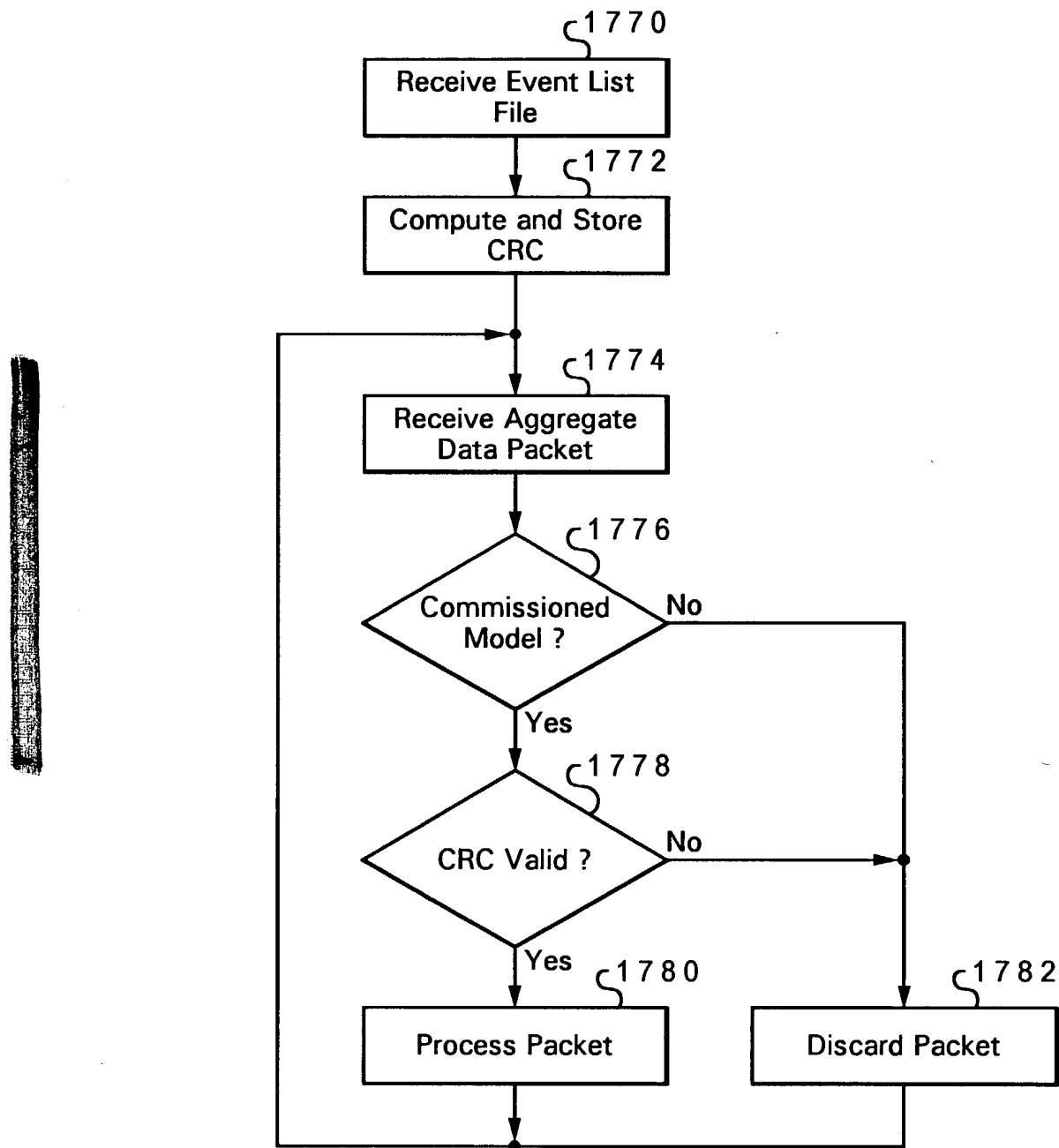


Fig. 17C

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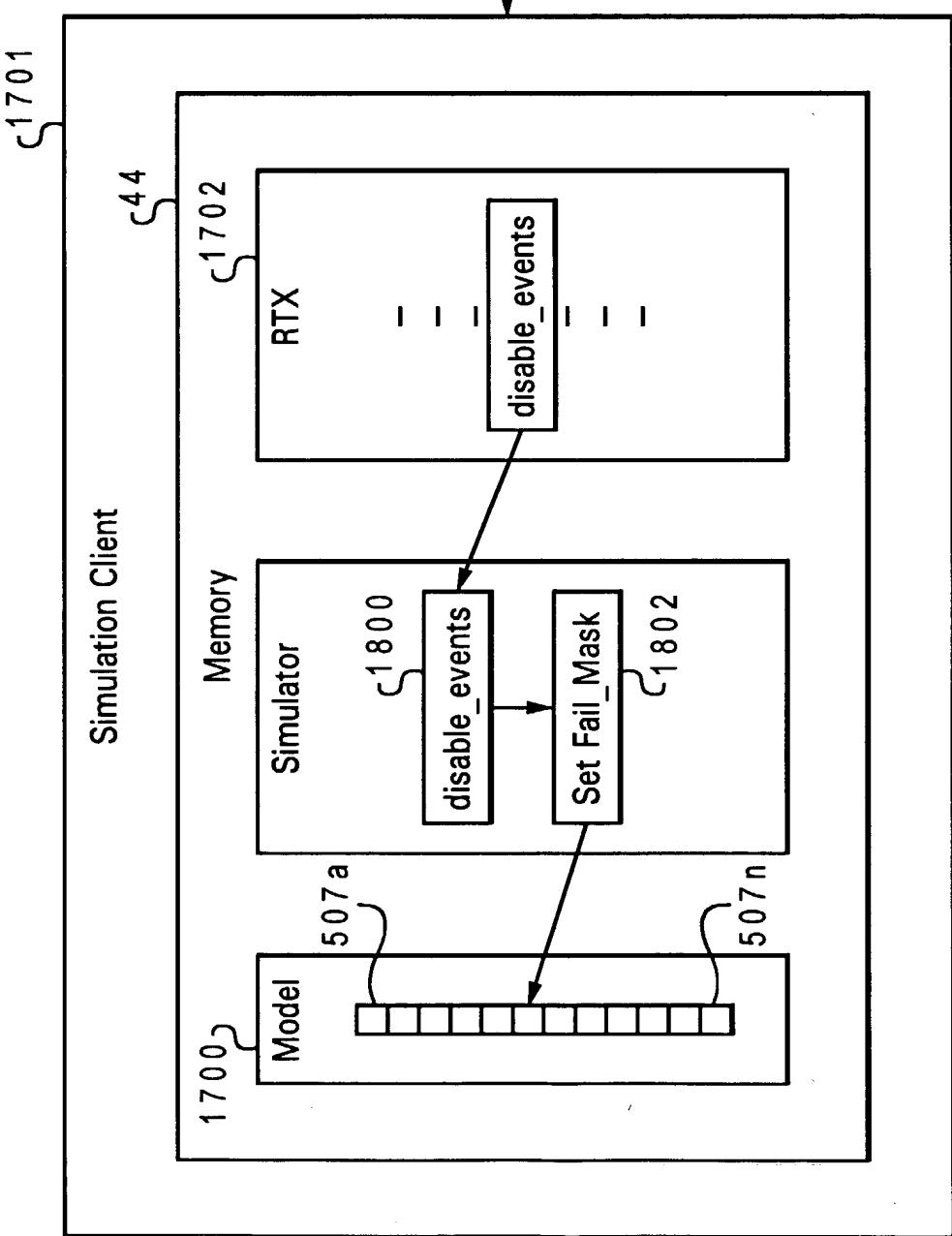
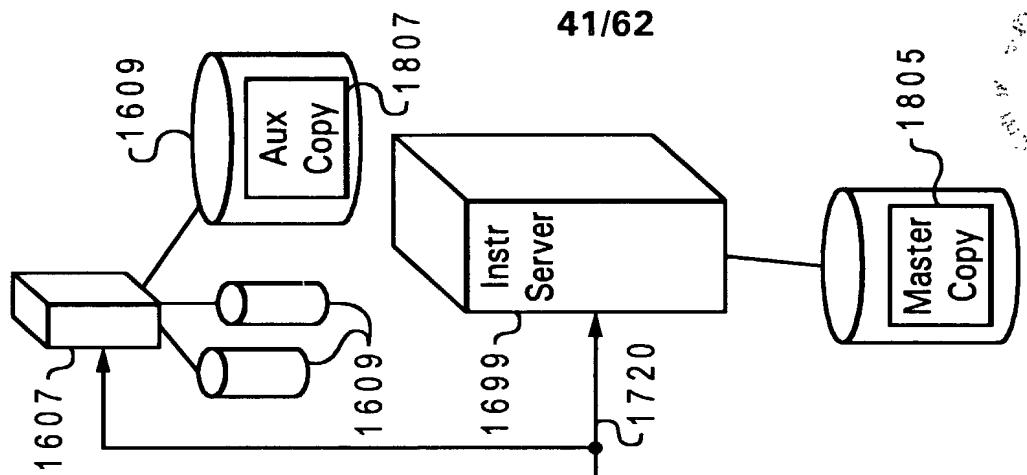
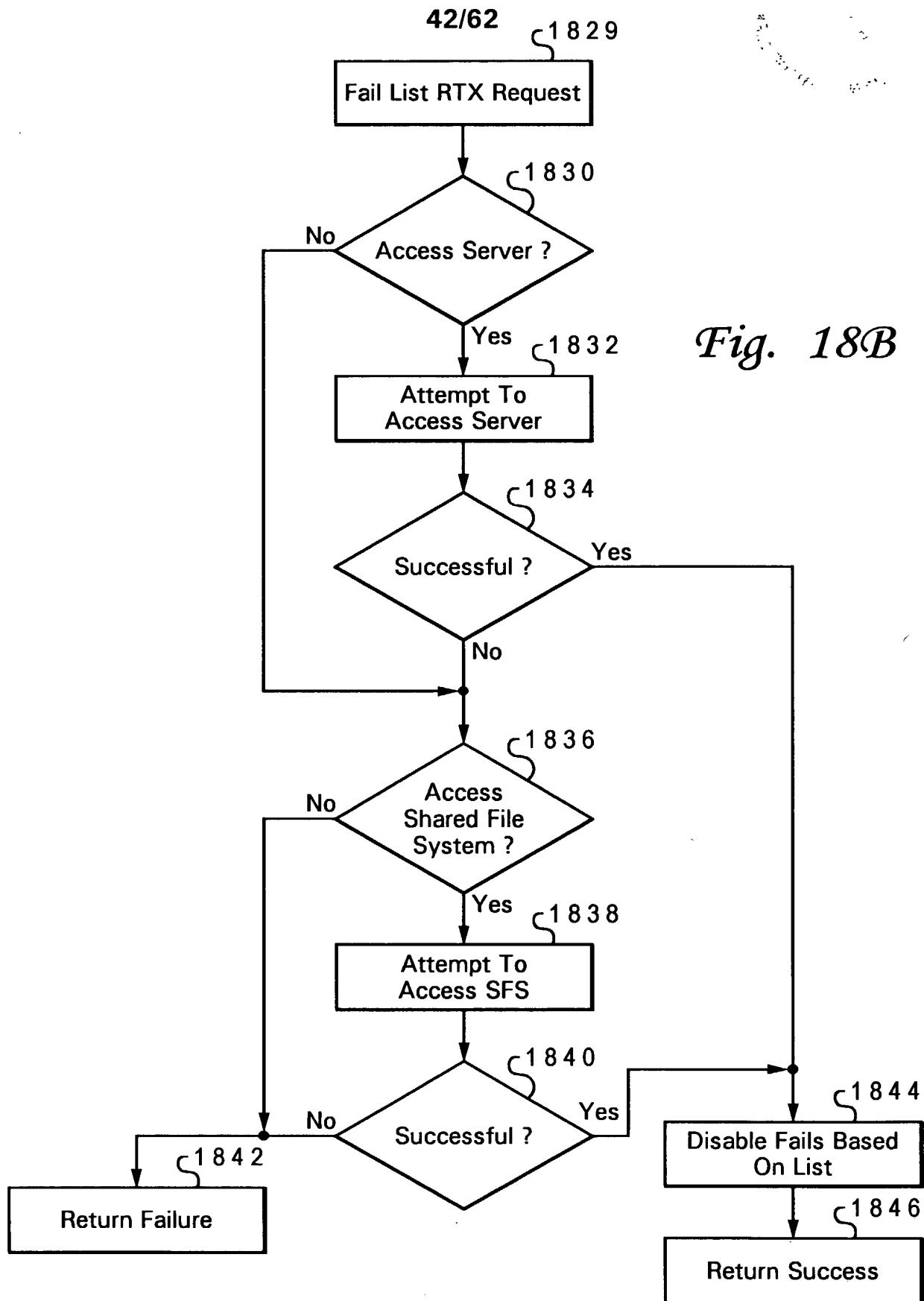


Fig. 18A

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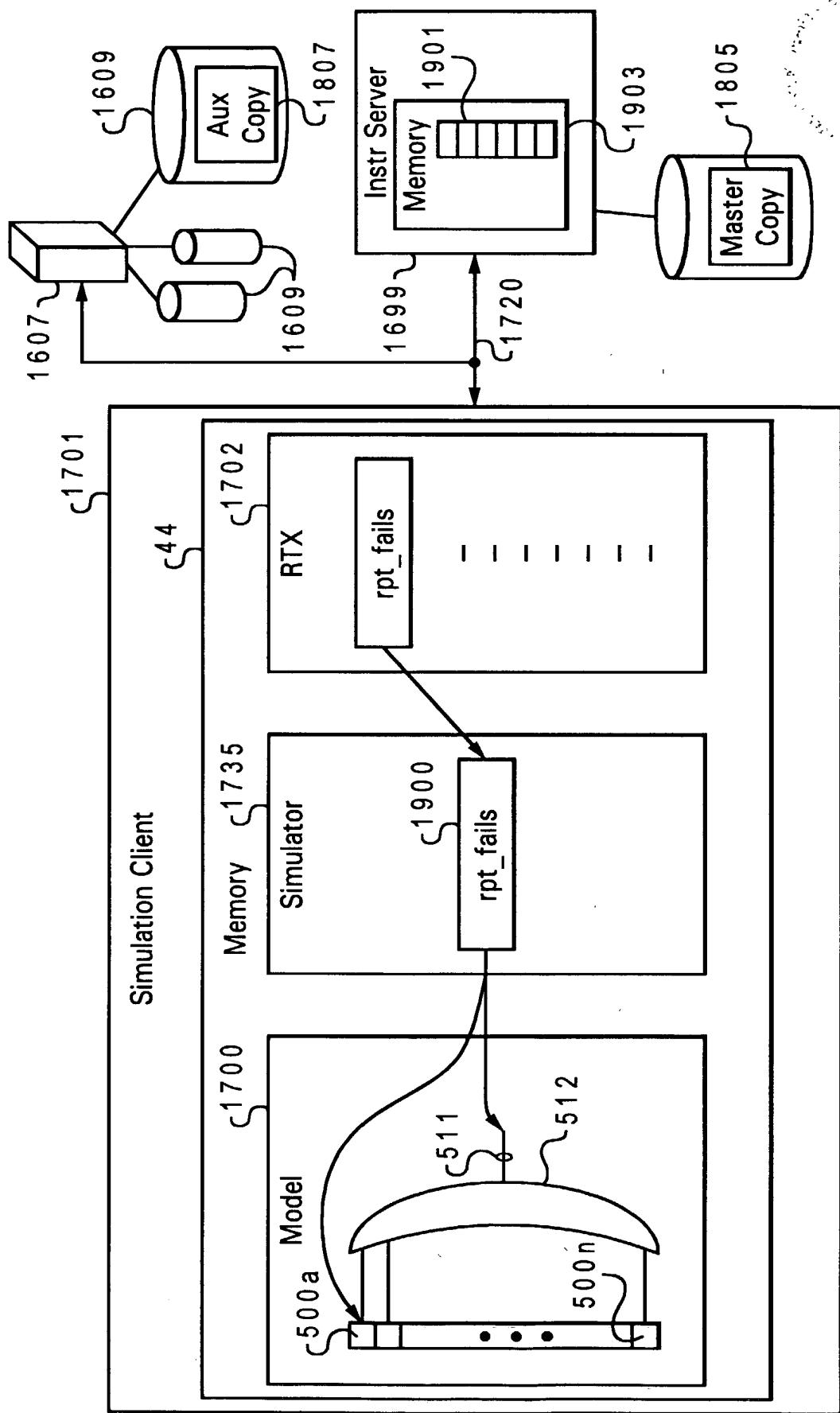


Fig. 19A

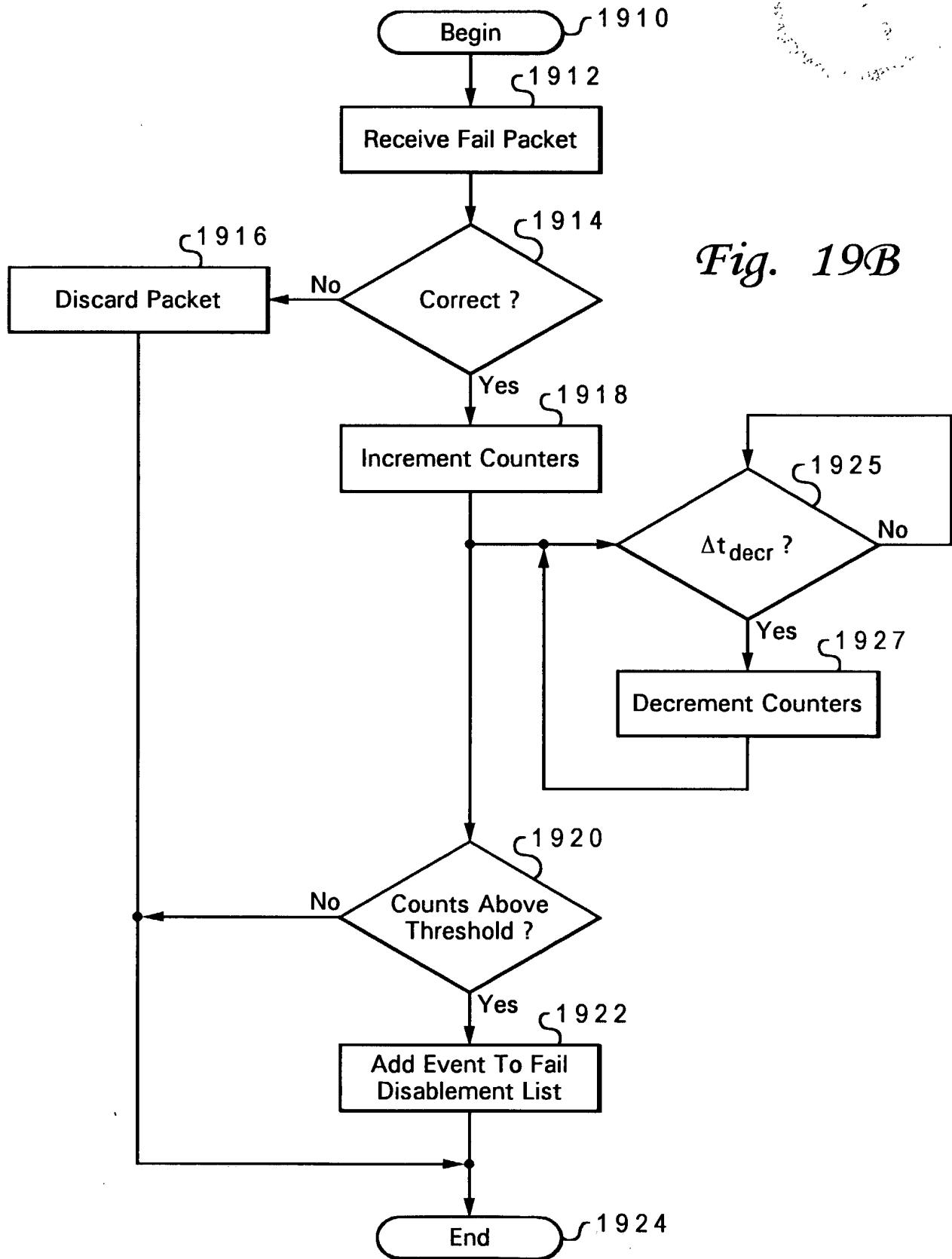


Fig. 19B

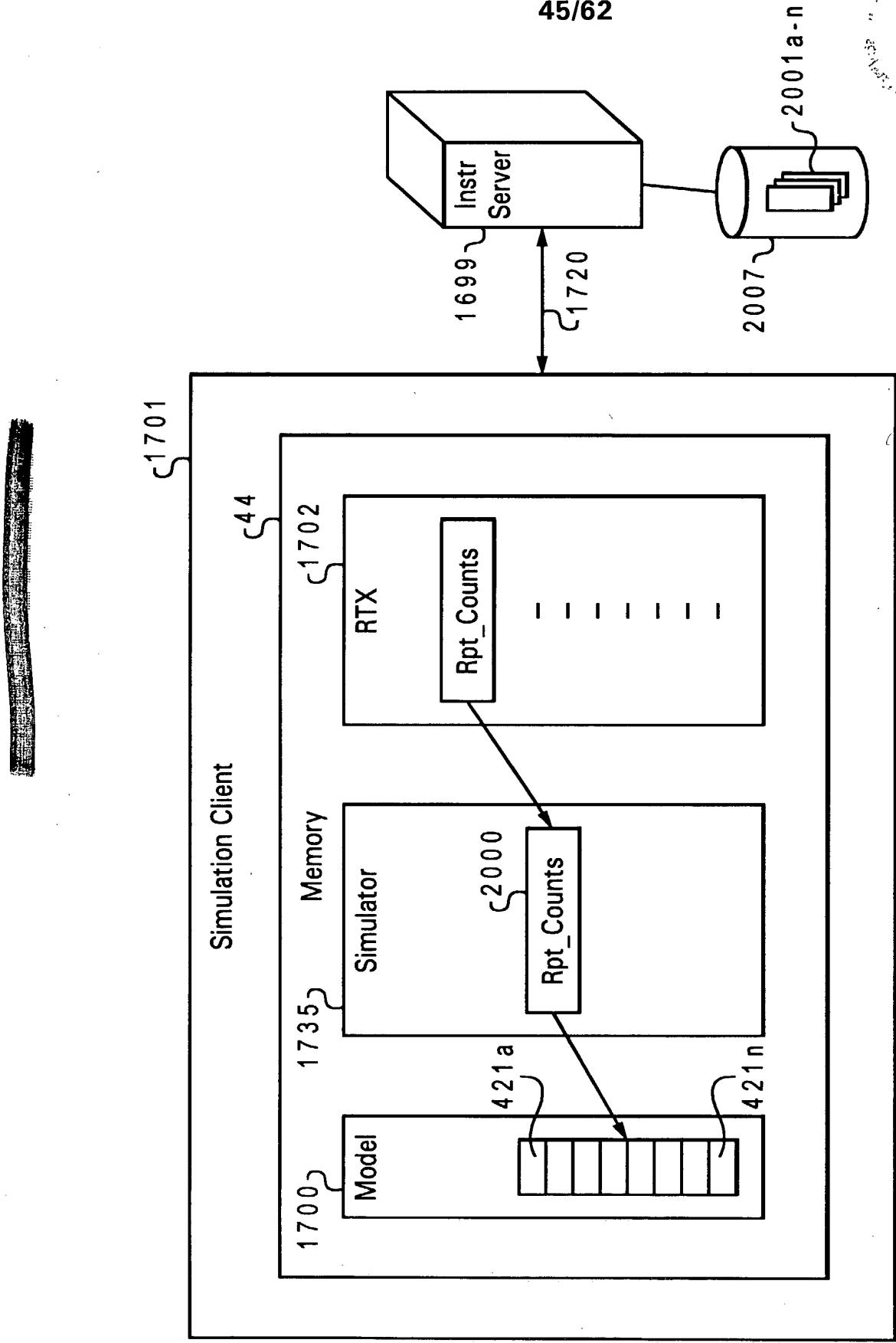


Fig. 20A

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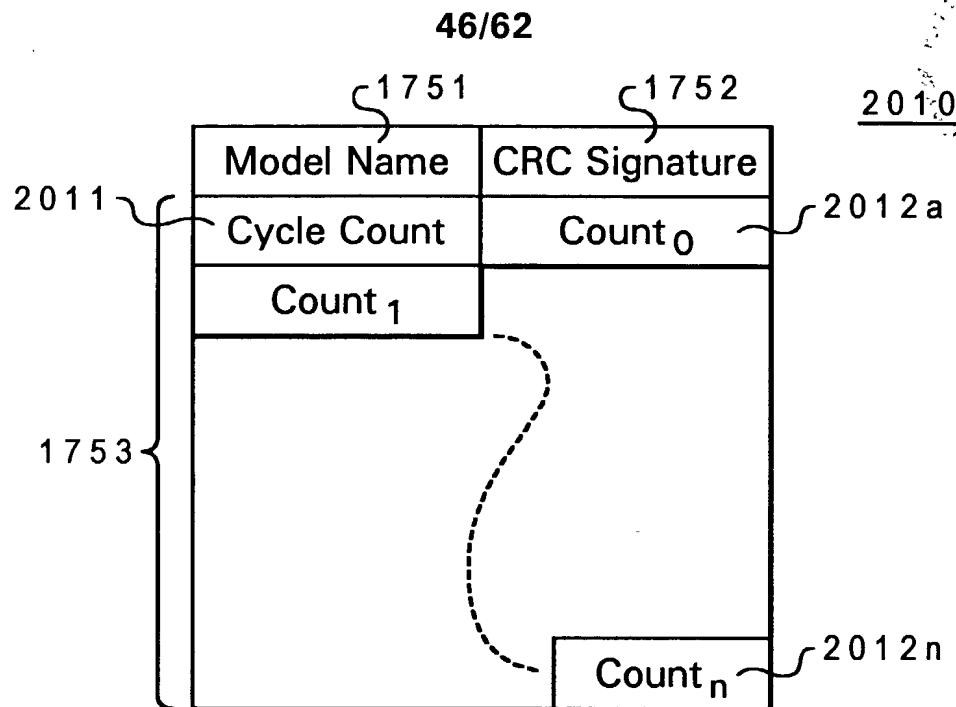


Fig. 20B

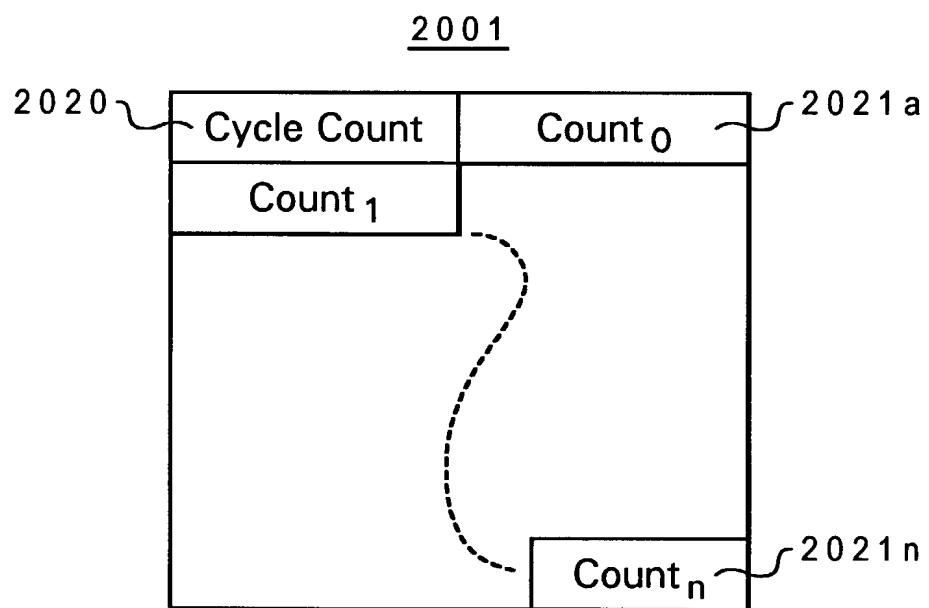


Fig. 20C

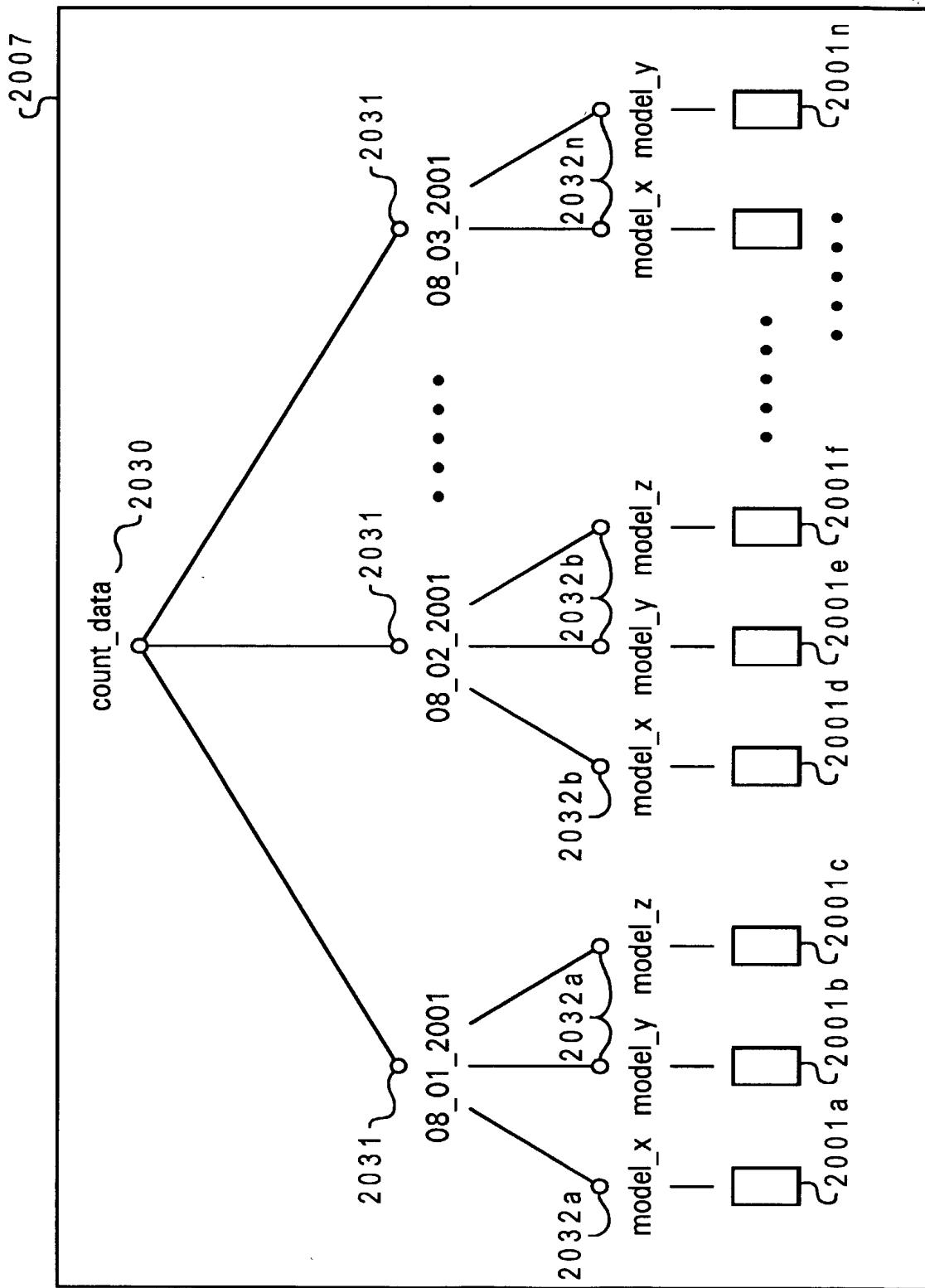


Fig. 20D

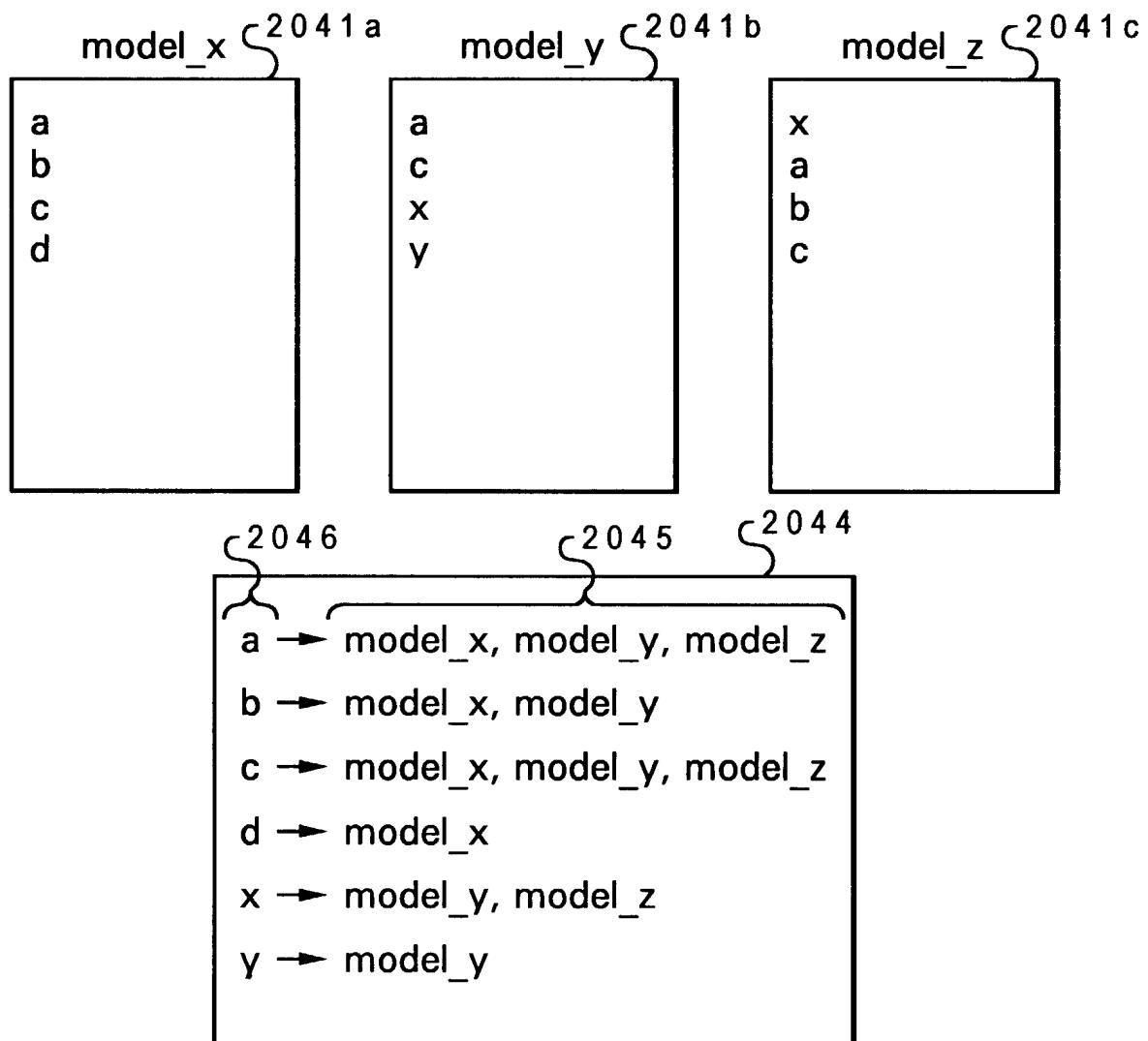


Fig. 20E

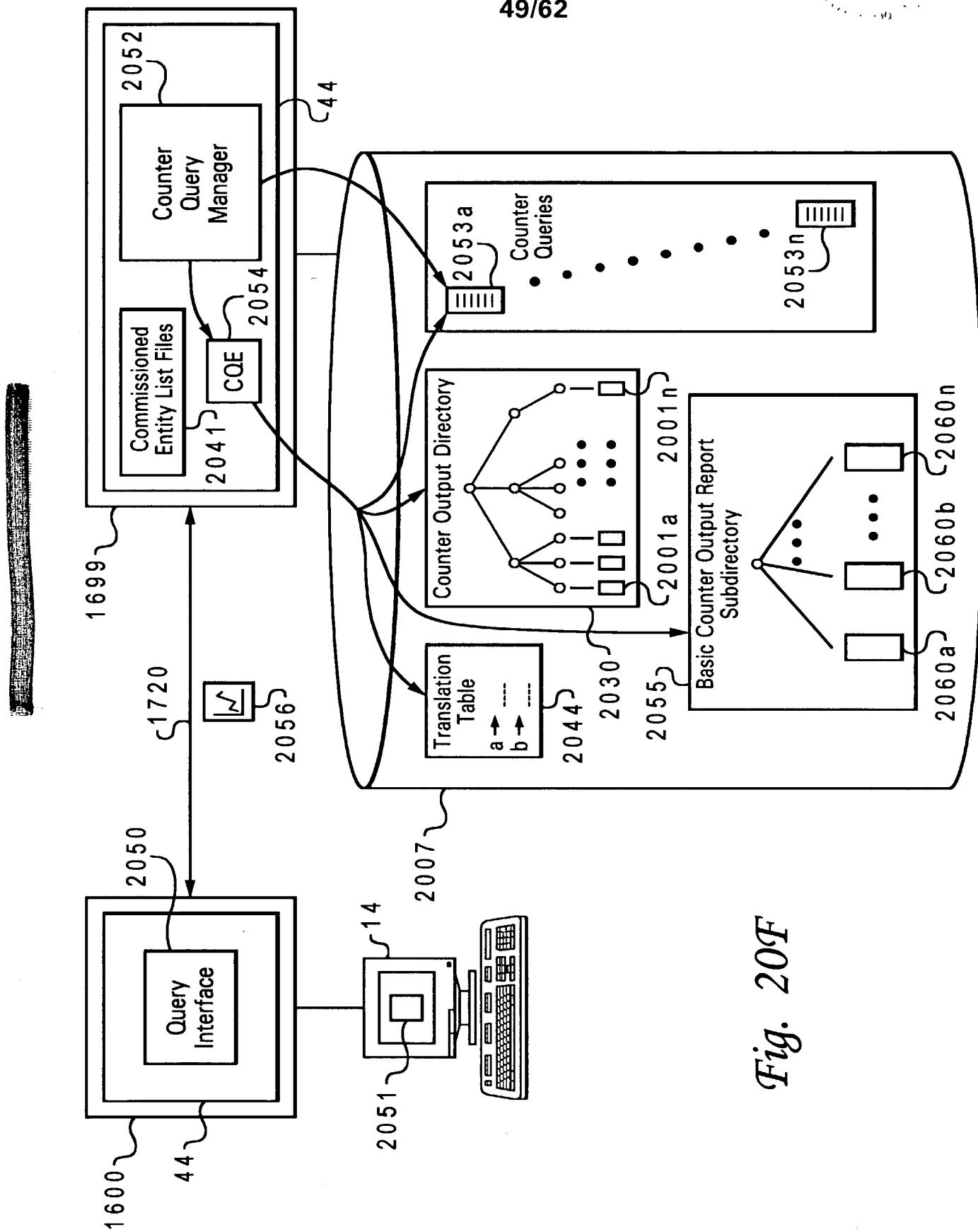


Fig. 20F

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2060	
8914	~ 2061
<X1.Z>.<B1>.<Z>.<count1>	57
<X1.Z>.<B2>.<Z>.<count1>	102
<X2.Z>.<B1>.<Z>.<count1>	1092
<X2.Z>.<B2>.<Z>.<count1>	16
<Y.Z>.<B1>.<Z>.<count1>	2921
<Y.Z>.<B2>.<Z>.<count1>	701
2063	
2064	

Fig. 20G

2065	
8914	
<B1>.<Z>.<count1>	4070
<B2>.<Z>.<count1>	819
2066	

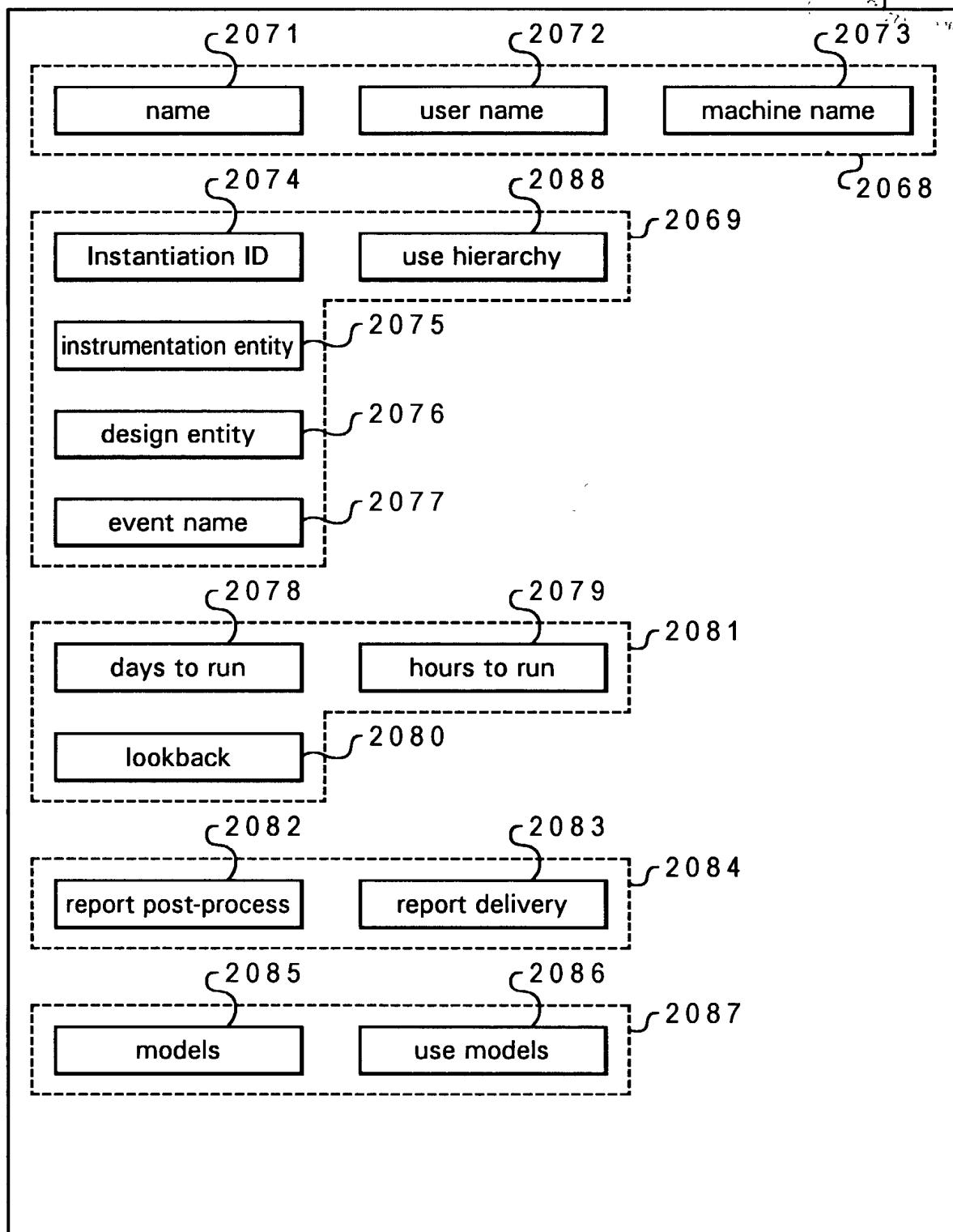


Fig. 20H

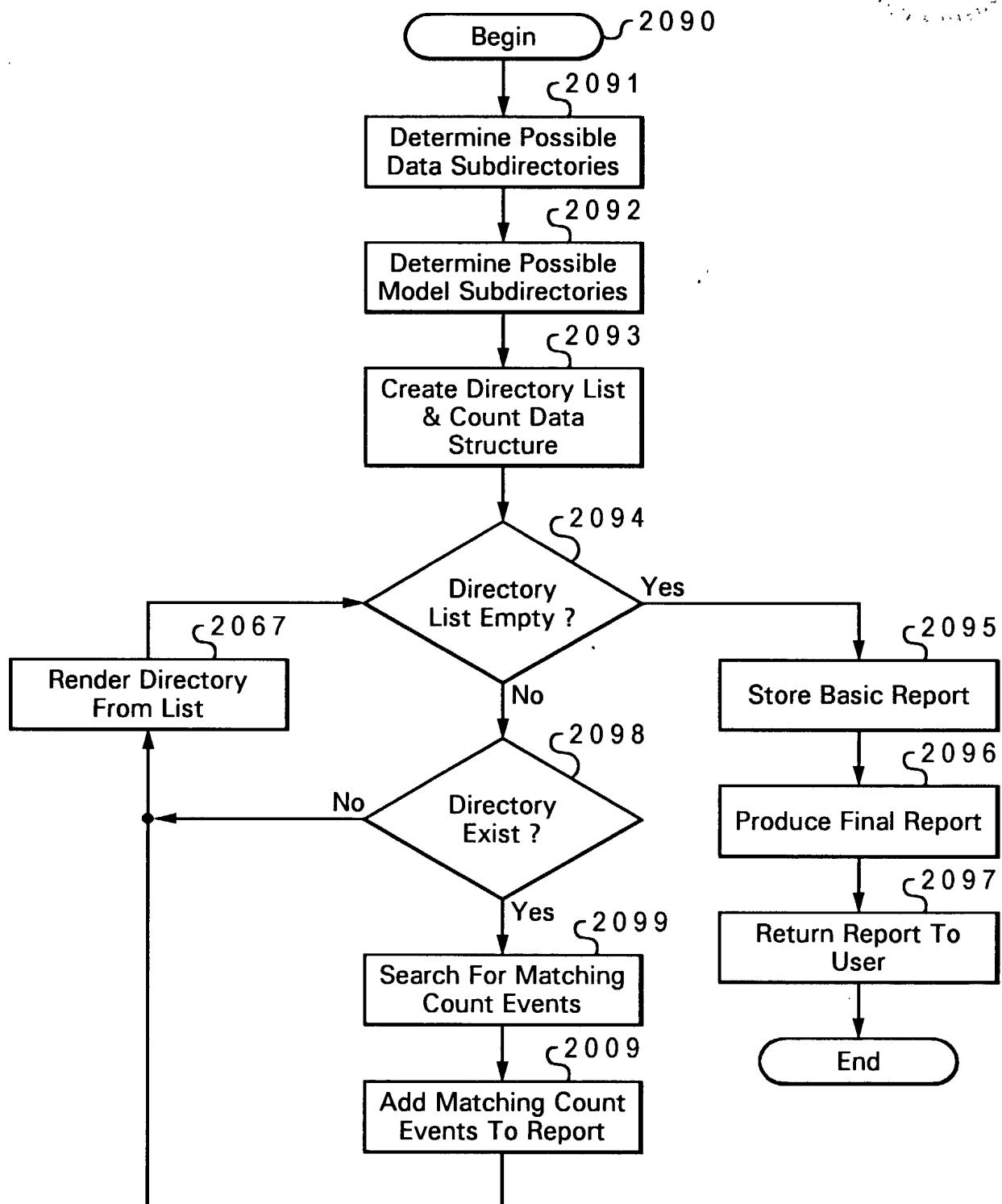


Fig. 20I

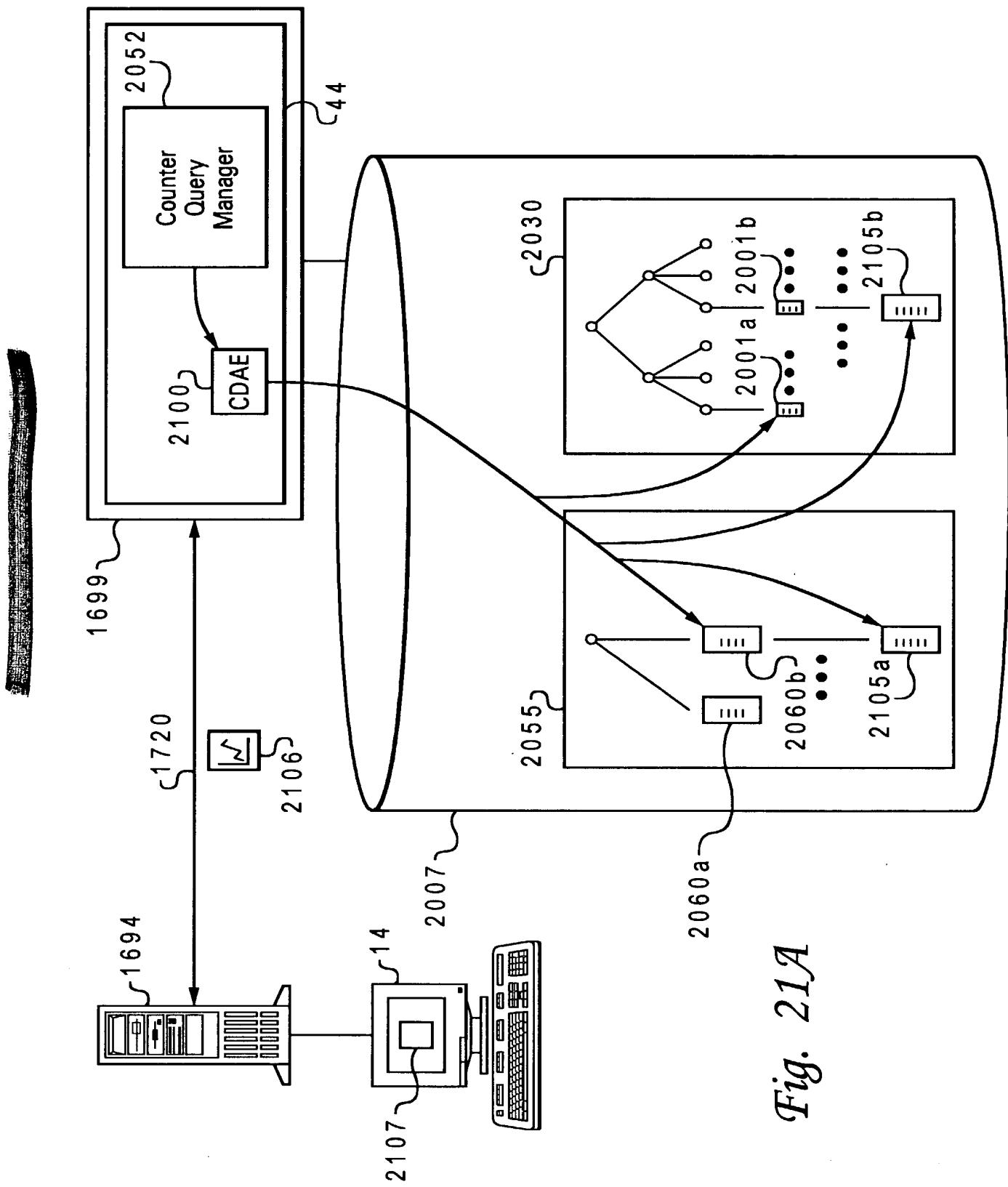


Fig. 21A

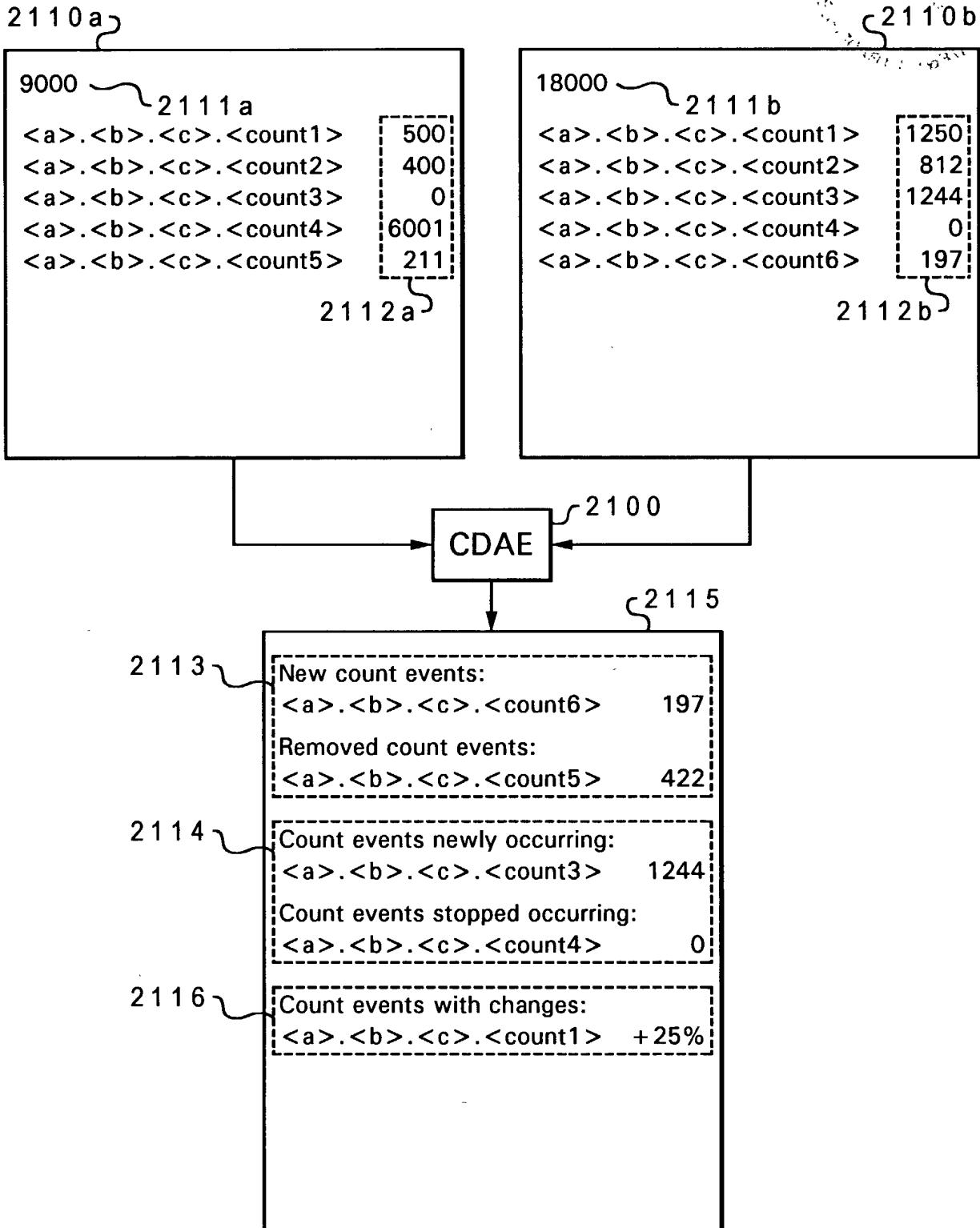


Fig. 21B

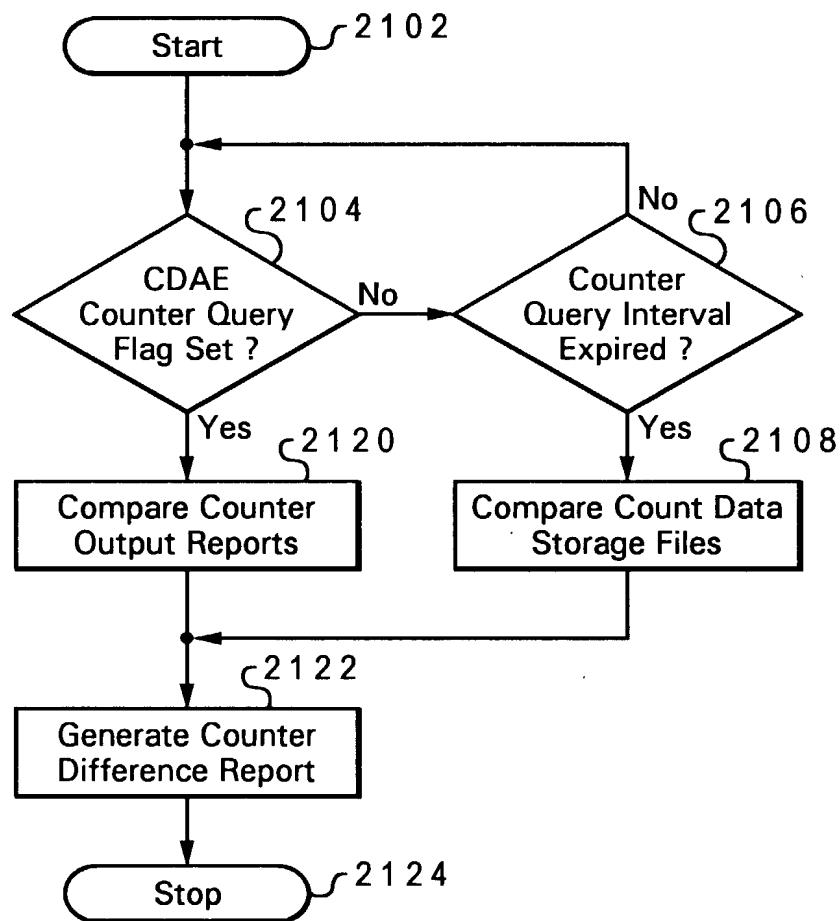


Fig. 21C

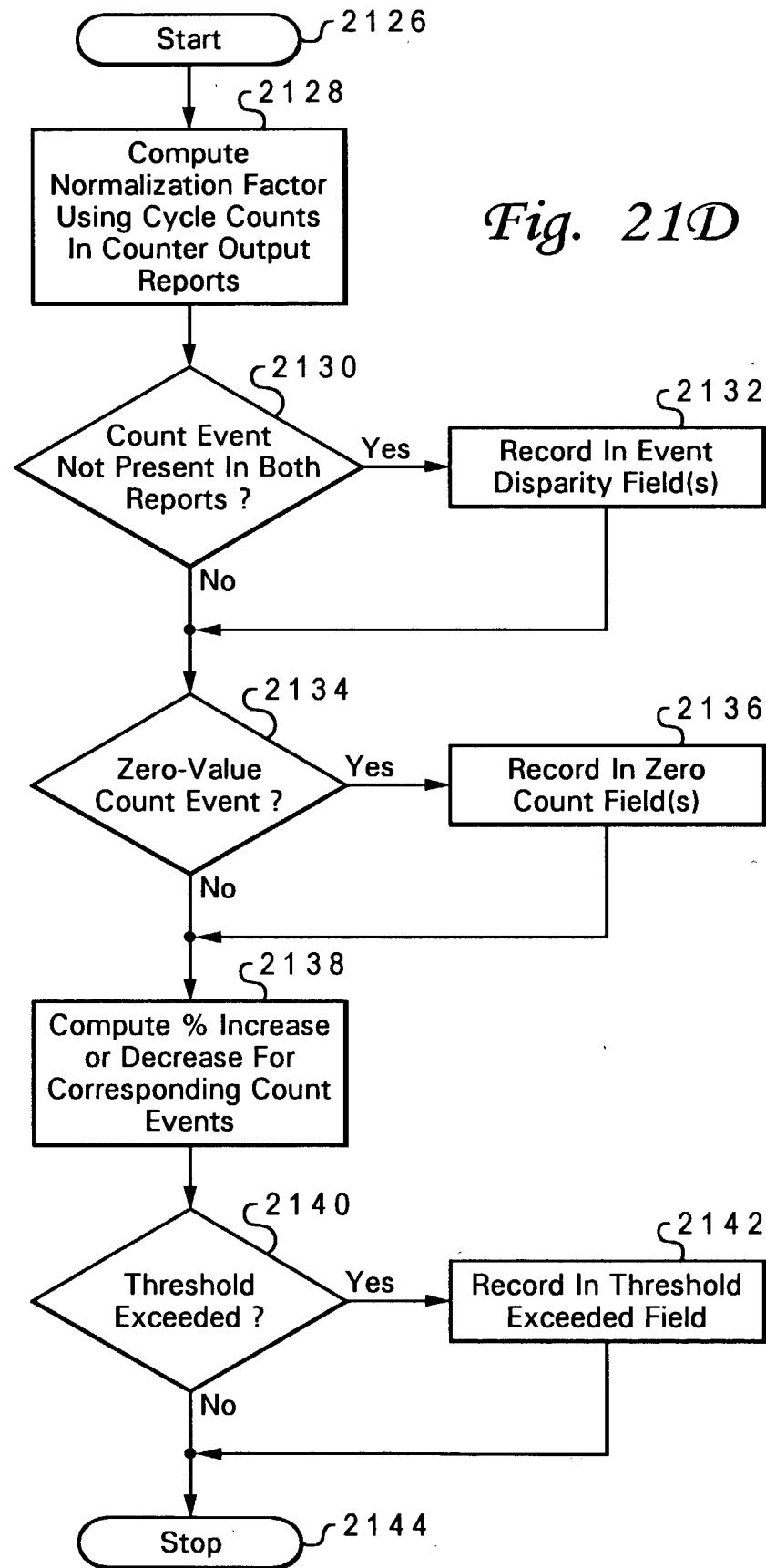
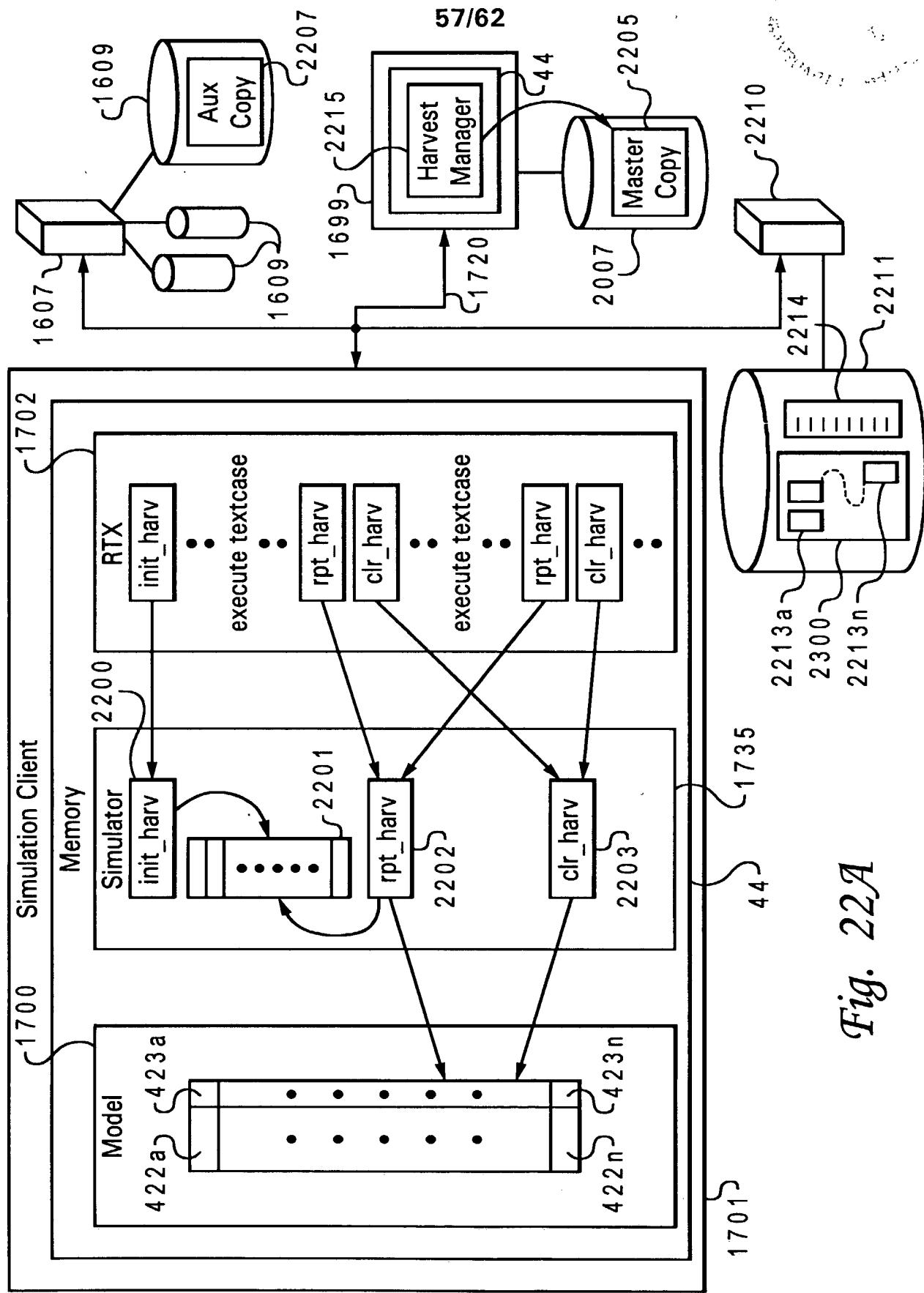


Fig. 21D

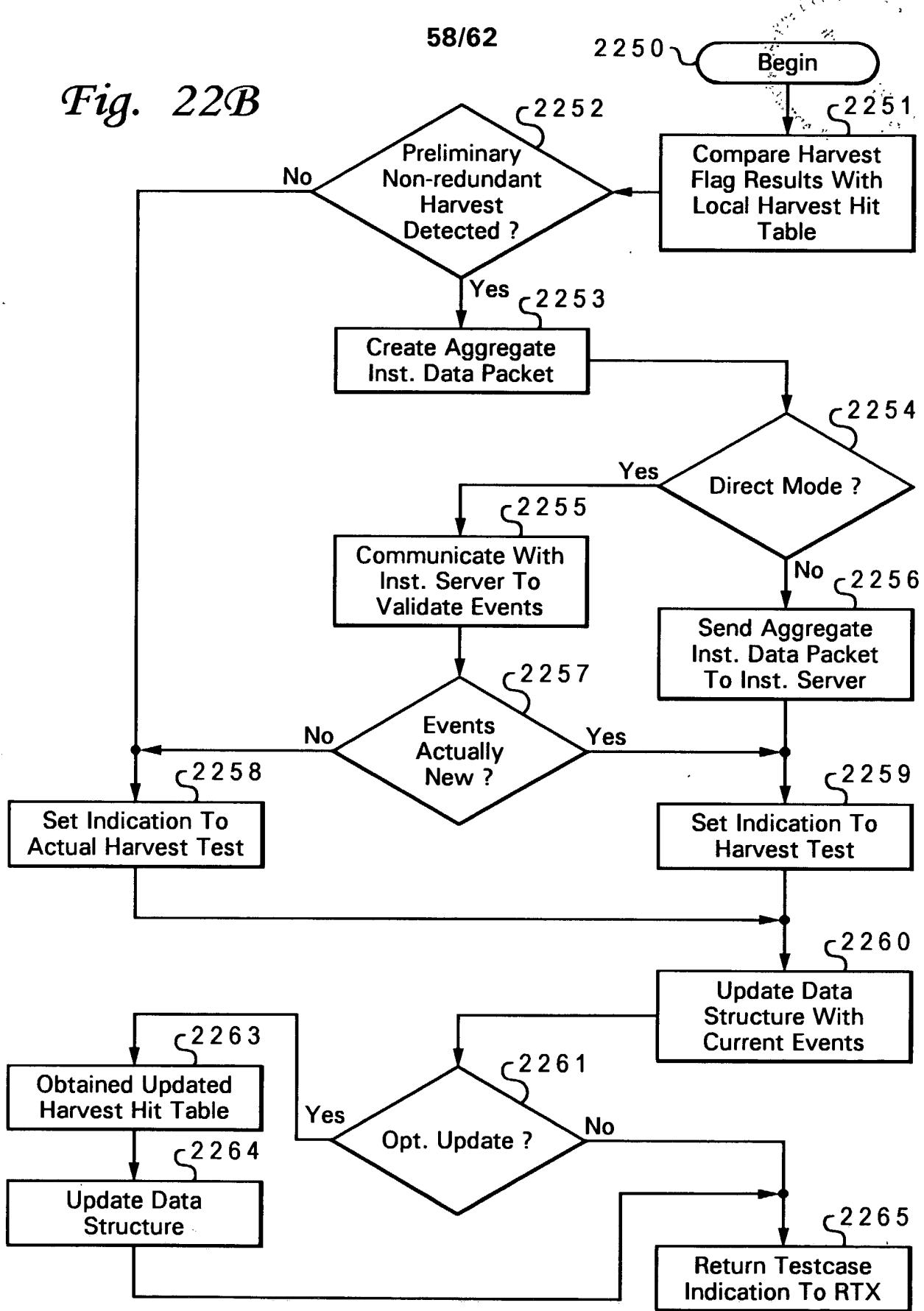
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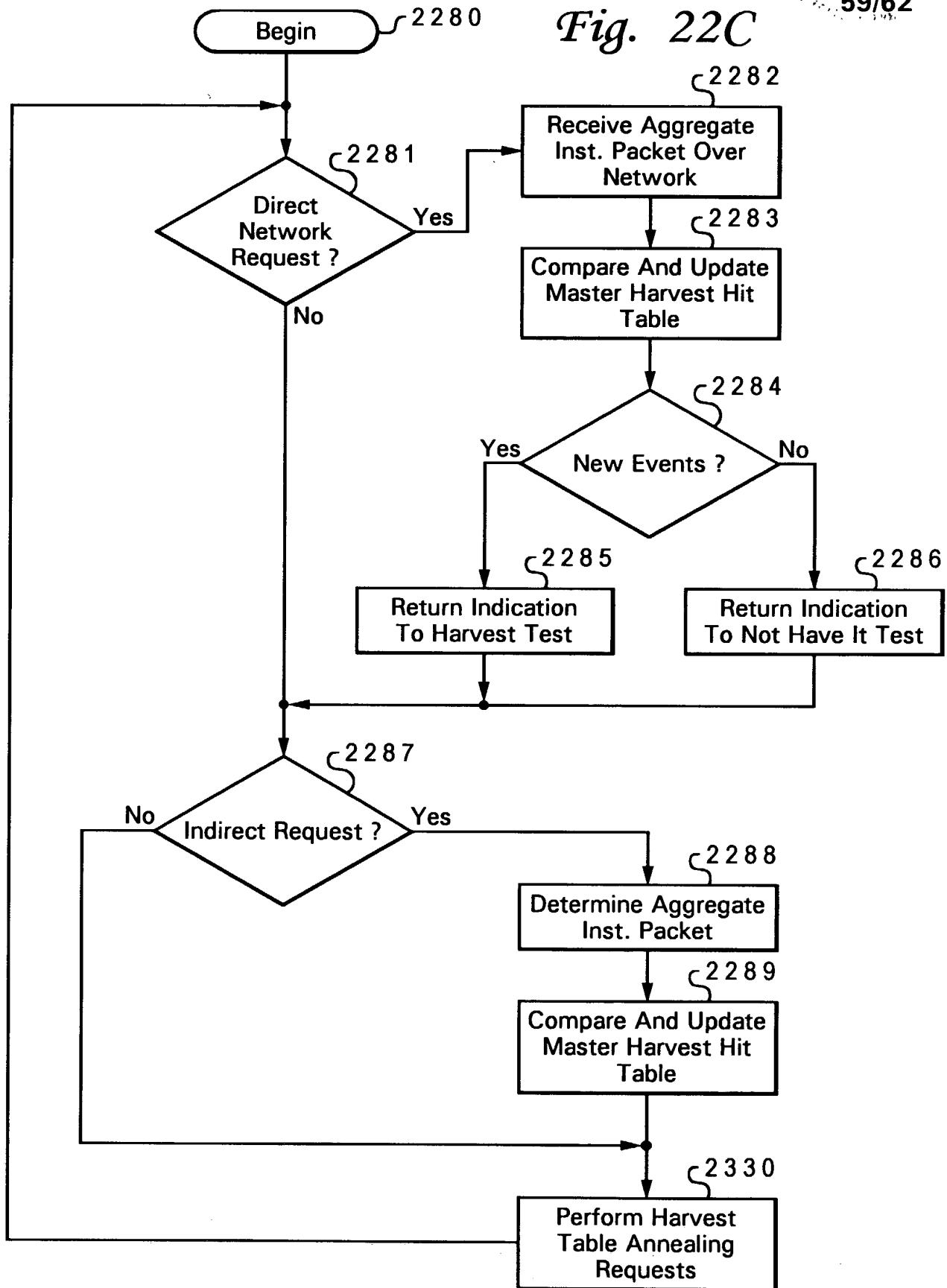


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Fig. 22B





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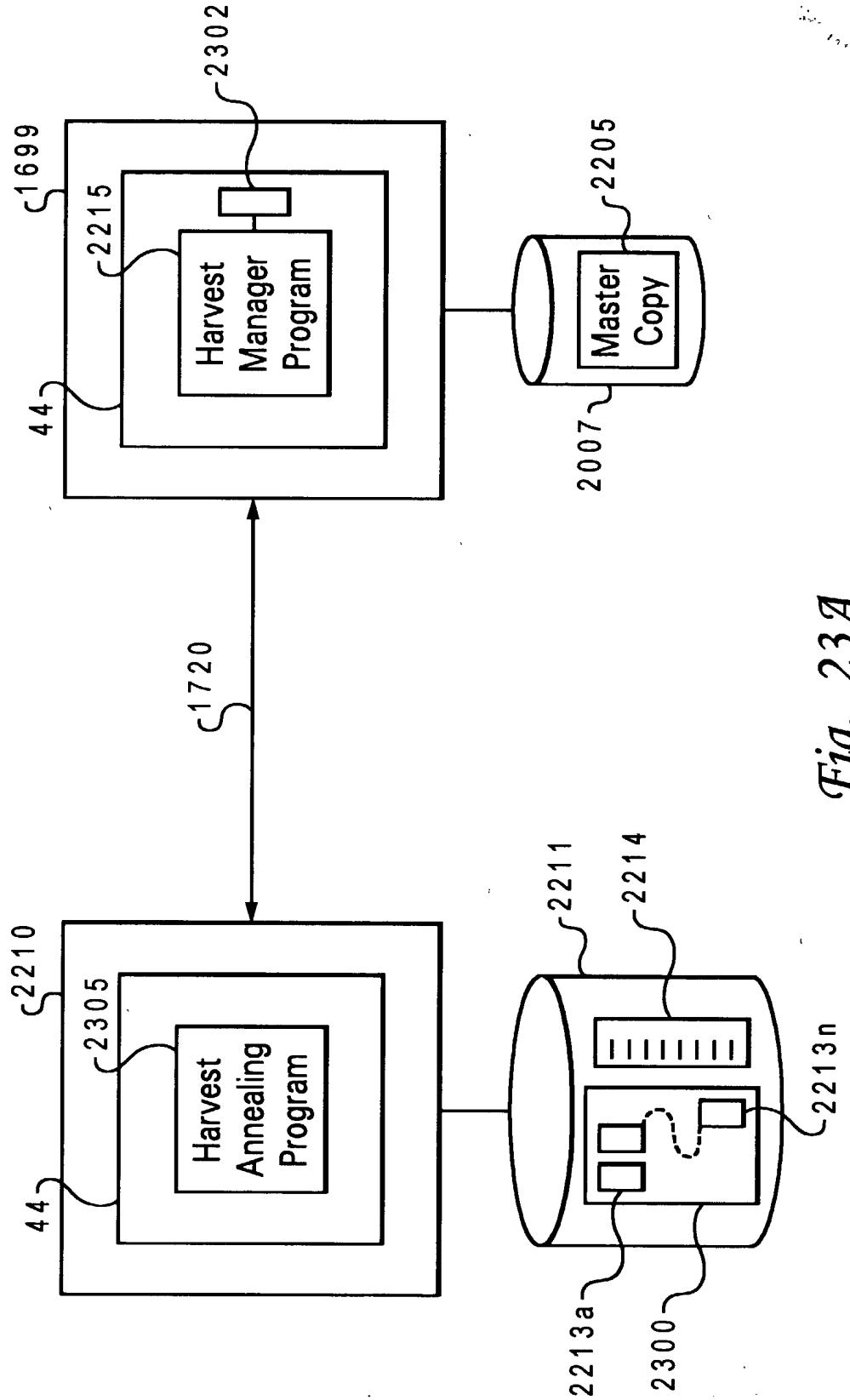


Fig. 23A

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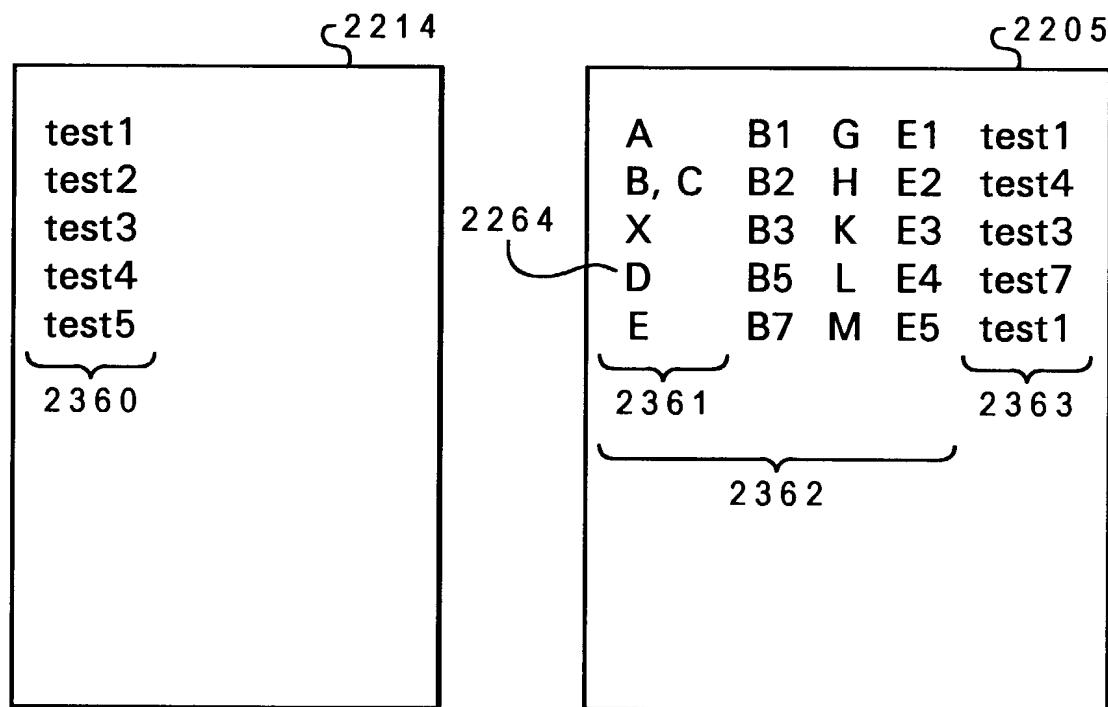


Fig. 23B

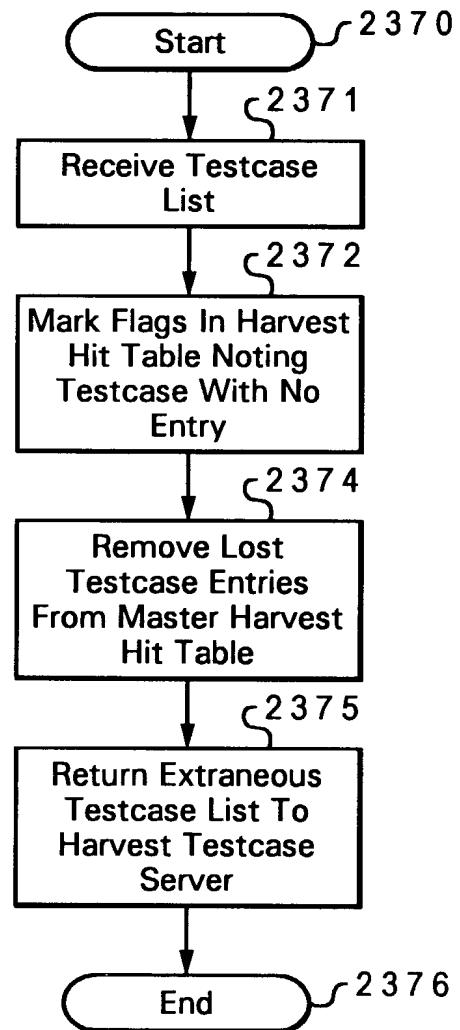


Fig. 23C